

3A 500V N Channel MOSFET

Features

- Low RDS(on)
- Low gate charge (typ. $Q_g = 7.2\text{nC}$)
- 100% UIS tested
- RoHS compliant

Applications

- Power factor correction.
- Switched mode power supplies.
- LED driver.

Descriptions

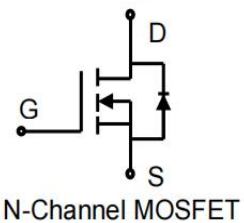
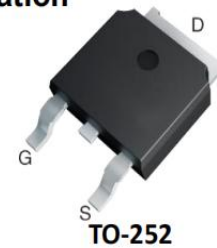
The Power MOSFET is fabricated using the advanced planar VDMOS technology.

The resulting device has low conduction resistance, superior switching performance and high avalanche energy.

Product Summary

V_{DSS}	500V
I_D	3A
$R_{DS(on),max}$	3.6 Ω
$Q_{g,typ}$	7.2nC

Pin Configuration



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	VDSS	500	V
Continuous drain current ¹⁾ (TC = 25°C) (TC = 100°C)	ID	3	A
		2	A
Pulsed drain current ²⁾	IDM	9	A
Gate-Source voltage	VGSS	±30	V
Avalanche energy, single pulse ³⁾	EAS	42	mJ
Power Dissipation	PD	60	W
Operating and Storage Temperature Range	TJ, TSTG	-55 to +150	°C
Continuous diode forward current	IS	3	A
Diode pulse current	IS,pulse	9	A

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R θ JC	2.1	°C/W
Thermal Resistance, Junction-to-Ambient, minimal footprint ⁴⁾	R θ JA	62	°C/W
Soldering temperature, wave soldering only allowed at leads. (1.6mm from case for 10s)	Tsold	260	°C

Electrical Characteristics(Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =0.25mA	400	-	-	V
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =0.25mA	2.0	-	4.0	V
Drain cut-off current	I _{DSS}	V _{DS} =500V, V _{GS} =0 V, T _j = 25°C	-	-	1	μA
Gate leakage current, Forward	I _{GSSF}	V _{GS} =30V, V _{DS} =0V	-	-	100	nA
Gate leakage current, Reverse	I _{GSSR}	V _{GS} =-30V, V _{DS} =0V	-	-	-100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10 V, I _D =1.5A T _j = 25°C T _j = 150°C	- -	3.0 7.0	3.6	Ω
Dynamic characteristics						
Input capacitance	C _{iss}	V _{DS} = 25V, V _{GS} = 0 V, f = 250kHz	-	276	-	pF
Output capacitance	C _{oss}		-	27.4	-	
Reverse transfer capacitance	C _{rss}		-	0.94	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 250V, I _D = 3A R _G = 10Ω, V _{GS} =10V	-	8.6	-	ns
Rise time	t _r		-	31	-	
Turn-off delay time	t _{d(off)}		-	12.5	-	
Fall time	t _f		-	8.3	-	
Gate charge characteristics						
Gate to source charge	Q _{gs}	V _{DD} =400V, I _D =3A V _{GS} =0 to 10V	-	1.5	-	nC
Gate to drain charge	Q _{gd}		-	3.8	-	
Gate charge total	Q _g		-	7.2	-	
Gate plateau voltage	V _{plateau}		-	5.5	-	V
Reverse diode characteristics						
Diode forward voltage	V _{SD}	V _{GS} =0V, I _F =3A	-	-	1.3	V
Reverse recovery time	t _{rr}	V _R =400V, I _F =3A, dI _F /dt=100 A/μs	-	209	-	ns
Reverse recovery charge	Q _{rr}		-	858	-	nC
Peak reverse recovery current	I _{rrm}		-	5.7	-	A

Notes:

1. Drain current limited by maximum junction temperature.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. I_{AS}=2.9A, L=10mH, V_{DD}=60V, Starting T_j= 25°C.
4. The value of R_{thJA} is measured by placing the device in a still air box which is one cubic foot.

Electrical Characteristic Curve (Tc=25° C unless otherwise noted)

Figure 1. Typ. Output Characteristics

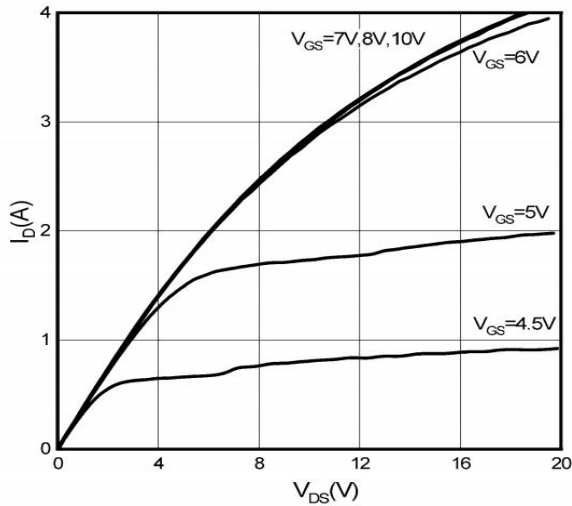


Figure 2. Transfer Characteristics

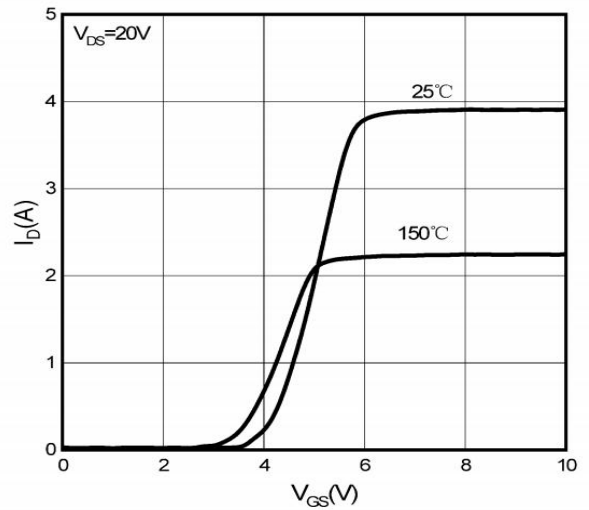


Figure 3. On-Resistance vs. Drain Current

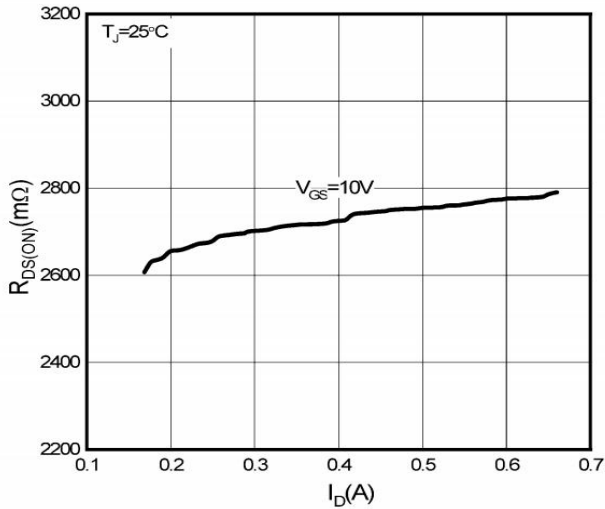


Figure 4. On-Resistance vs. Temperature

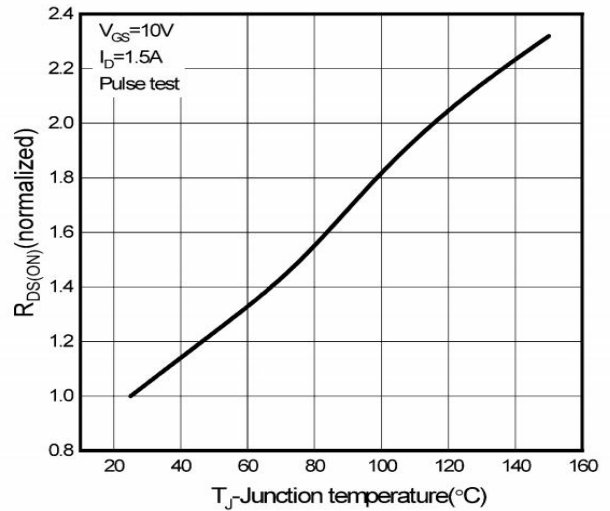


Figure 5. Breakdown Voltage vs. Temperature

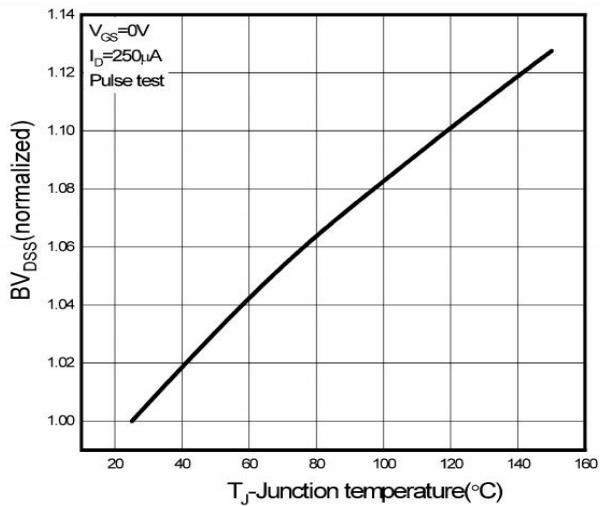
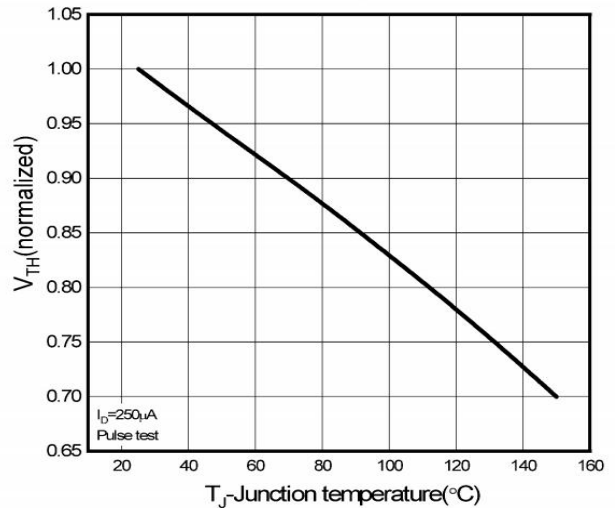


Figure 6. Threshold Voltage vs. Temperature



Electrical Characteristic Curve (Tc=25° C unless otherwise noted)

Figure 7. R_{DS(on)} vs. Gate Voltage

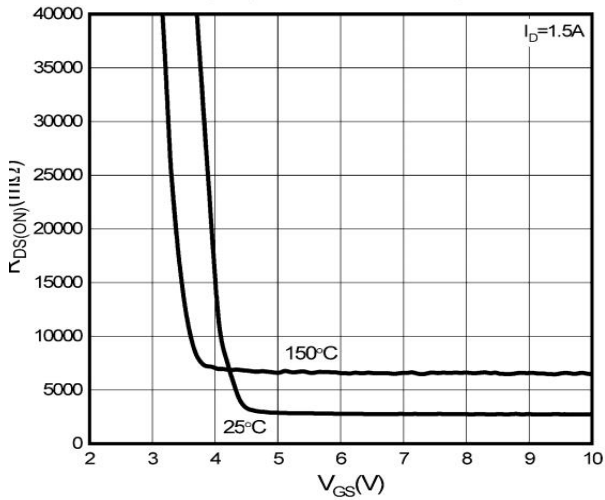


Figure 8. Body-Diode Characteristics

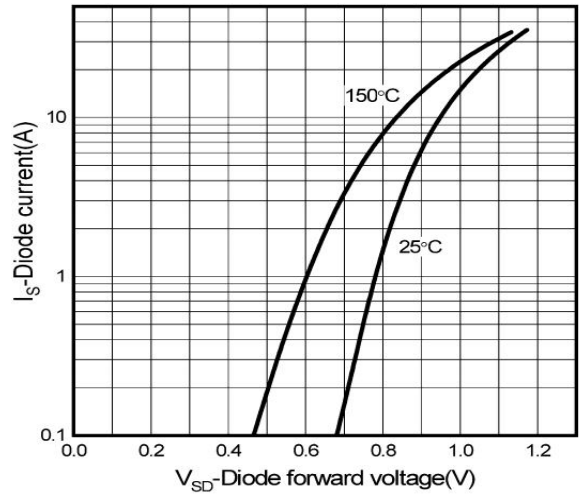


Figure 9. Capacitance Characteristics

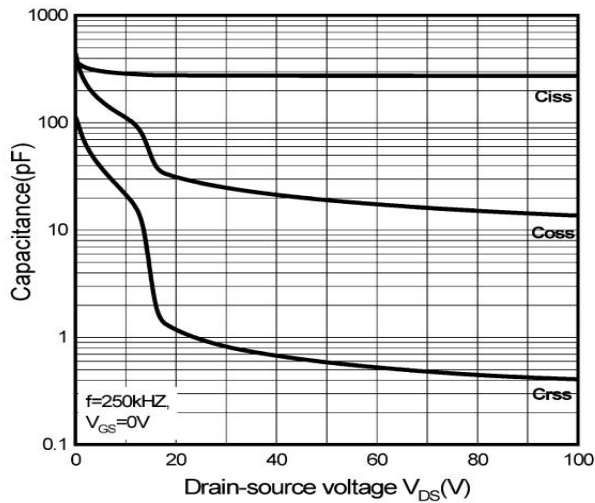


Figure 10. Gate Charge Characteristics

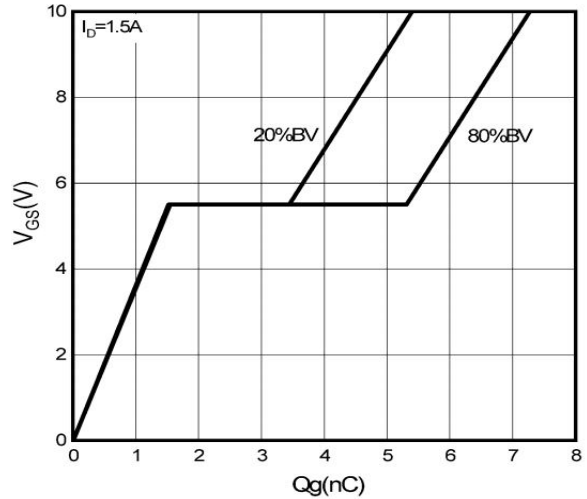


Figure 11. Drain Current Derating

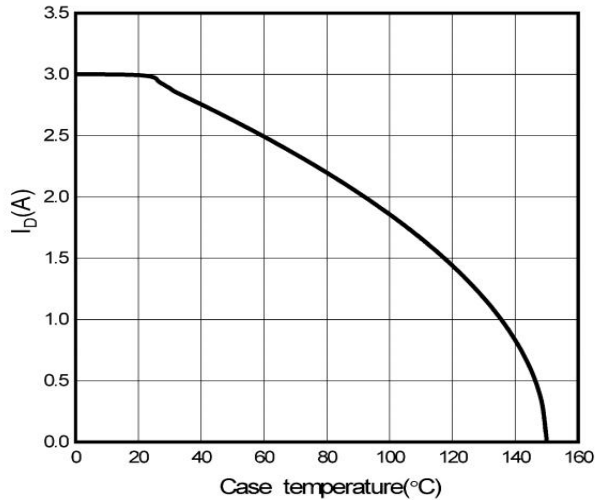
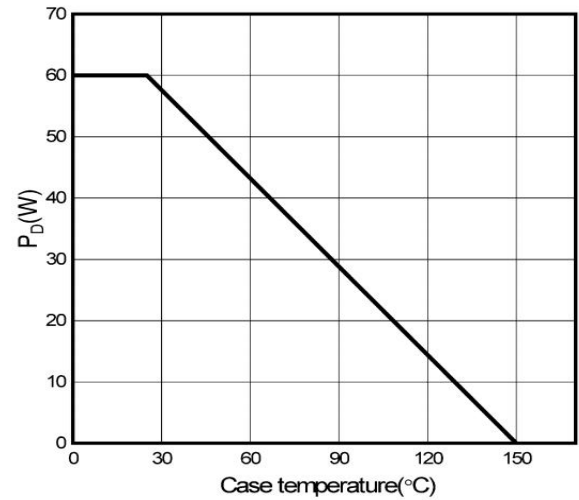


Figure 12. Power Dissipation vs. Temperature



Electrical Characteristic Curve (Tc=25° C unless otherwise noted)

Figure 13. Safe Operating Area

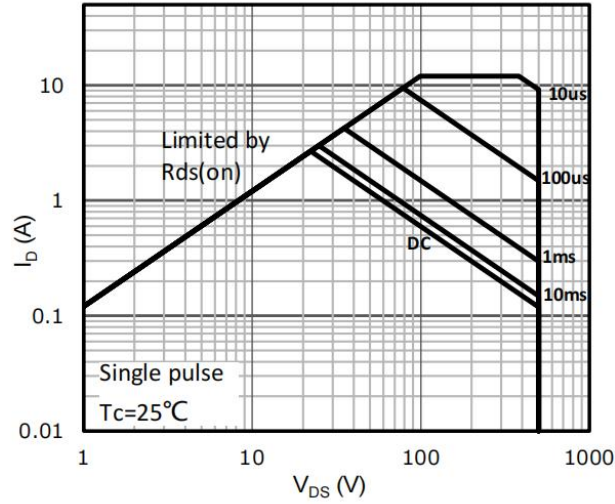
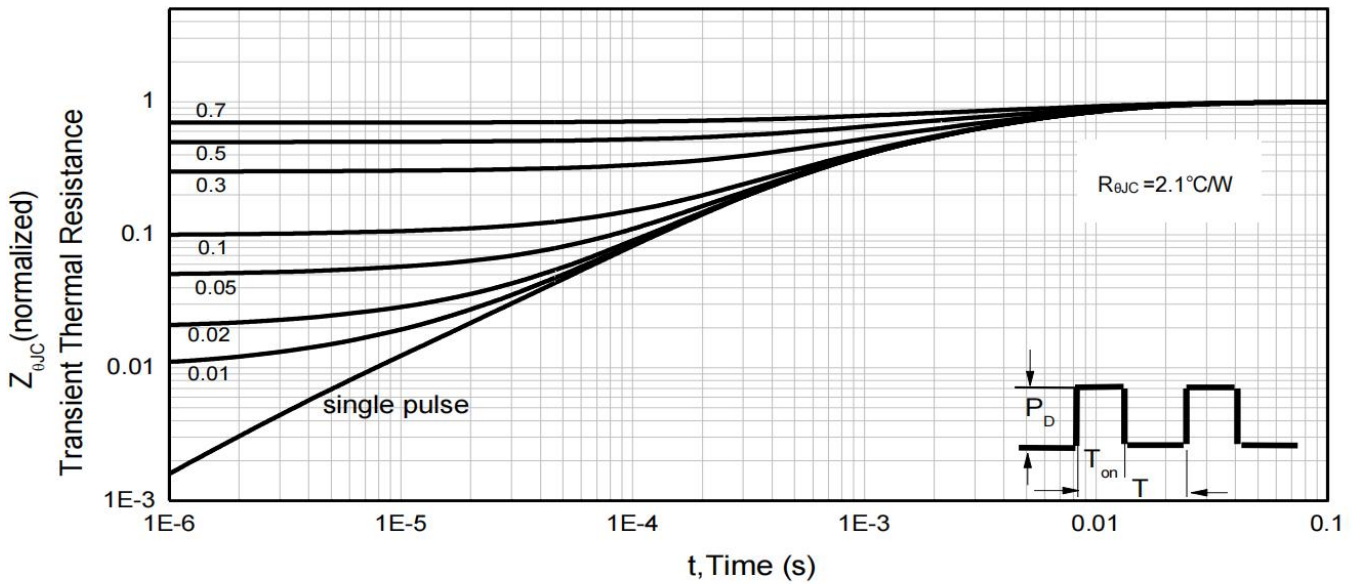
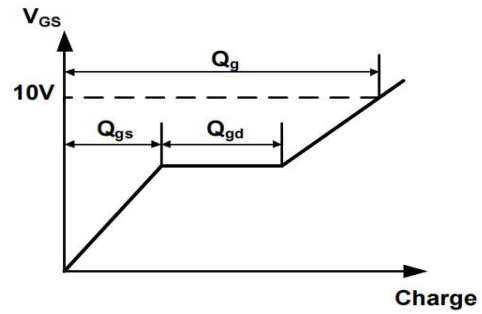
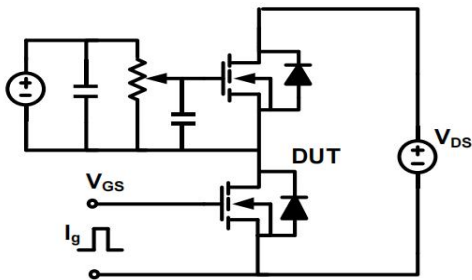


Figure 14. Normalized Maximum Transient Thermal Impedance (R_{thJC})

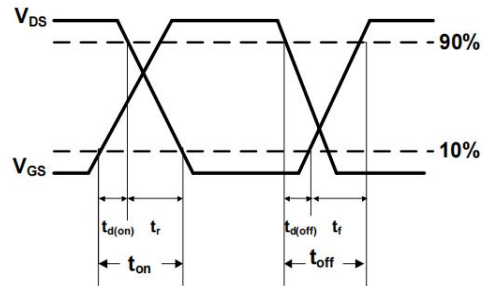
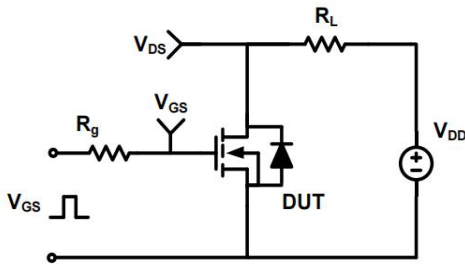


Test Circuit & Waveforms

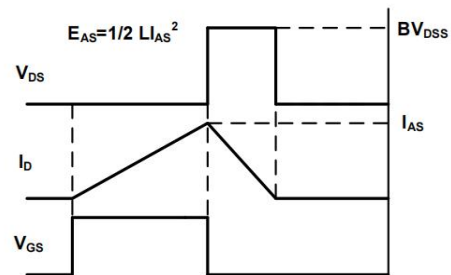
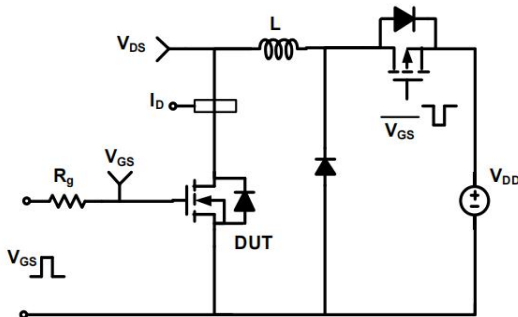
Gate Charge Test Circuit & Waveform



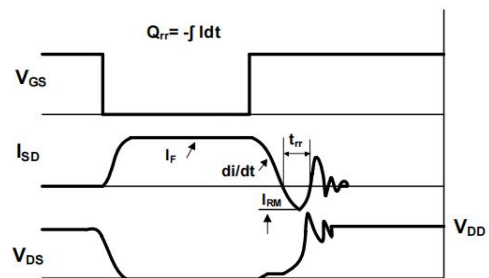
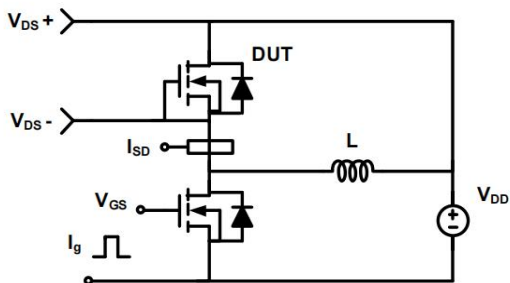
Resistive Switching Test Circuit & Waveform



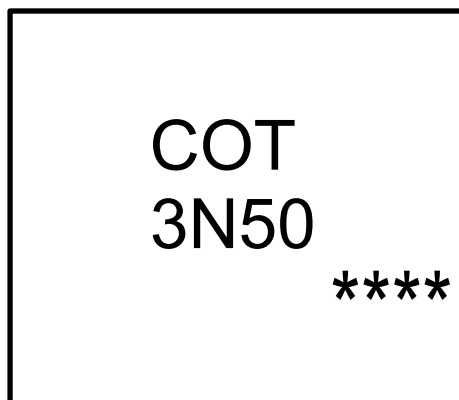
Unclamped Inductive Switching (UIS) Test Circuit & Waveform



Diode Recovery Test Circuit & Waveform



Marking Instructions



Note:

COT: Company Logo

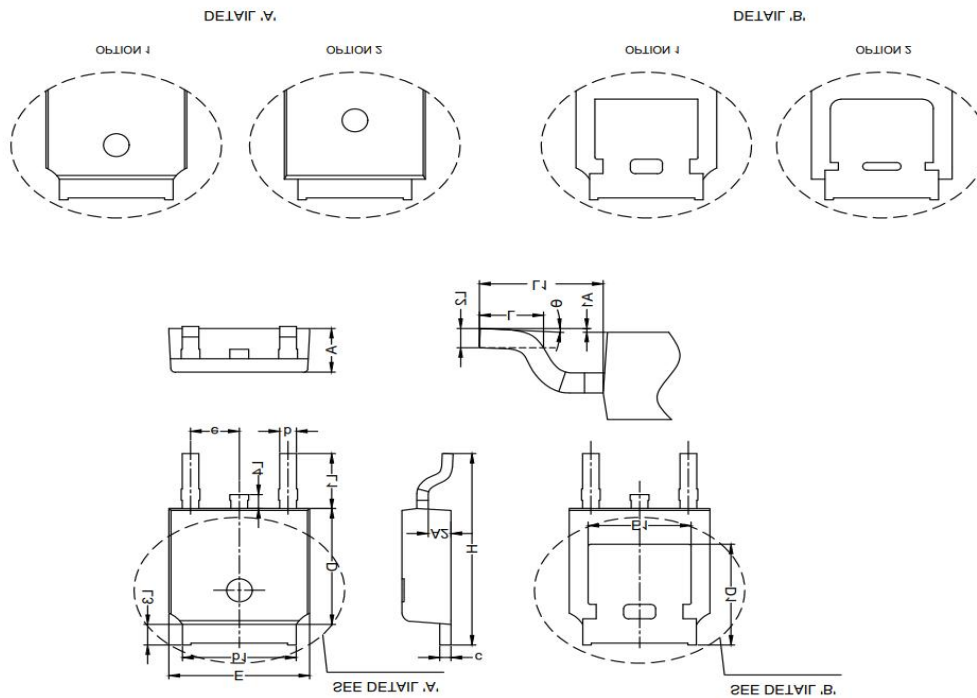
3N50: Product Type.

****: Lot No. Code, code change with Lot No.

Package Marking and Ordering Information

Device	Device Package	Marking	Units/Reel
CT3N50D	TO-252	3N50	2500

Package Outline Dimensions



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.10	2.50	0.083	0.098
A1	0.00	0.20	0.000	0.008
A2	0.85	1.17	0.033	0.046
b	0.60	0.90	0.024	0.035
b1	4.95	5.48	0.195	0.216
c	0.41	0.61	0.016	0.024
D	5.95	6.35	0.234	0.250
D1	5.21	-	0.205	-
E	6.35	6.80	0.250	0.268
E1	4.32	-	0.170	-
e	2.286 BSC		0.090 BSC	
H	9.40	10.50	0.370	0.413
L	0.95	1.78	0.037	0.070
L1	2.90 REF		0.114 REF	
L2	0.51 BSC		0.020 BSC	
L3	0.88	1.28	0.035	0.050
L4	-	1.02	-	0.040
θ	0°	10°	0°	10°