Descriptions

This 100V 15A N-channel enhancement mode field effect transistor in a TO-252 plastic package.

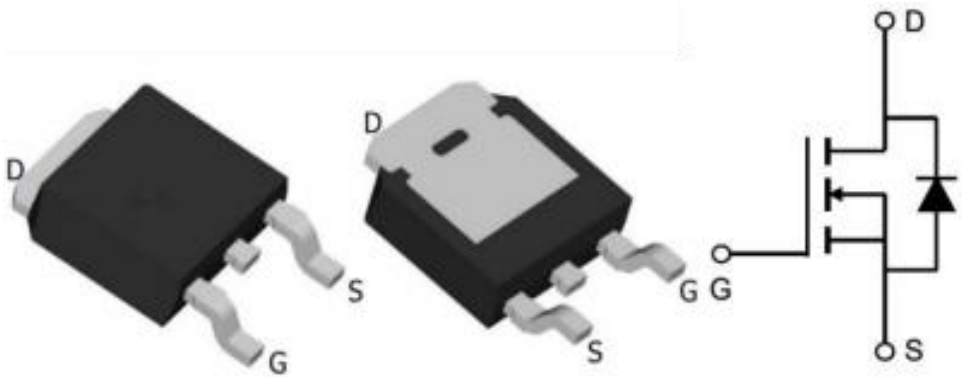
Features

- Advanced trench cell design
- Low Thermal Resistance
- Low Gate Charge
- 100% EAS Test,100% Rg Test
- Halogen-Free & Lead-Free

Application

- Motor/Body Load Control
- Load Switch
- PWM Application
- DC-DC converters

Equivalent Circuit & Pinning



Marking

See Marking Instructions

Absolute Maximum Ratings(Ta=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	VDS	100	V
Gate-Source Voltage	VGS	±20	V
Continuous Drain Current	ID	15	A
Peak Drain Current, Pulsed 1)	IDM	40	A
Avalanche Current	IAS	8	A
Single Pulse Avalanche Energy 2)	EAS	3.2	mJ
Power Dissipation Tc = 25℃	Ptot	30	W
Operating Junction and Storage Temperature Range	TJ, Tstg	-55~175	℃

Thermal Characteristics

Parameter	Symbol	Max	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	5	℃/W
Thermal Resistance from Junction to Ambient 3)	$R_{\theta JA}$	60	℃/W

Note：

1) Pulse Test: Pulse Width ≤ 100μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature TJ(MAX) = 150°C.

2) Limited by TJ(MAX), starting TJ = 25 °C, L = 0.1mH, Rg = 25 Ω, ID = 8 A, VGS = 10 V.

3) Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Characteristics at Ta = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 250 μA	BV_{DSS}	100			V
Drain-Source Leakage Current at V_{DS} = 40 V	I_{DSS}			1	μA
Gate Leakage Current at V_{GS} = ± 20 V	I_{GSS}			±100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 μA	$V_{GS(th)}$	1.2	1.9	2.5	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 5 A at V_{GS} = 4.5 V, I_D = 3 A	$R_{DS(on)}$		65 75	85 110	mΩ
DYNAMIC PARAMETERS					
Gate resistance at V_{DS} = 0 V, f = 1 MHz	R_g		7		Ω
Forward Transconductance at V_{DS} = 5 V, I_D = 20 A	g_{fs}		14		S
Input Capacitance at V_{GS} = 0 V, V_{DS} = 30 V, f= 1 MHz	C_{iss}		435		pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz	C_{oss}		45		pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz	C_{rss}		30		pF
Gate charge total at V_{DS} = 50 V, I_D = 1 V, V_{GS} = 10 V	Qg		9		nC
Gate to Source Charge at V_{DS} = 50 V, I_D = 1 V, V_{GS} = 10 V	Q_{gs}		1.7		nC
Gate to Drain Charge at V_{DS} = 50 V, I_D = 1 V, V_{GS} = 10 V	Q_{gd}		1.6		nC
Turn-On Delay Time at V_{GS} =4.5 V, V_{DD} = 30 V, I_D = 1 A, R_g = 6.8 Ω	$t_{d(on)}$		6		nS
Turn-On Rise Time at V_{GS} =4.5 V, V_{DD} = 30 V, I_D = 1 A, R_g = 6.8 Ω	t_r		15		nS
Turn-Off Delay Time at V_{GS} =4.5 V, V_{DD} = 30 V, I_D = 1 A, R_g = 6.8 Ω	$t_{d(off)}$		16		nS
Turn-Off Fall Time at V_{GS} =4.5 V, V_{DD} = 30 V, I_D = 1 A, R_g = 6.8 Ω	t_f		10		nS
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_{SD} = 8 A, V_{GS} = 0 V	V_{SD}		0.85	1.2	V
Body Diode Reverse Recovery Time at I_F = 20 A, di/dt = 500 A / μs	t_{rr}		18.5		nS
Body Diode Reverse Recovery Charge at I_F = 20 A, di/dt = 500 A / μs	Q_{rr}		50		nC

Electrical Characteristics Curves

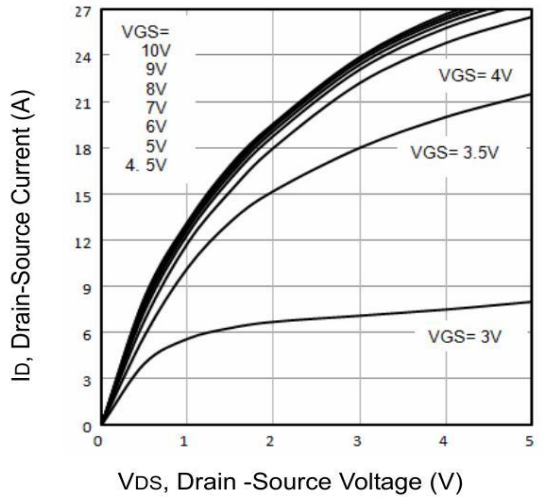


Fig1. Typical Output Characteristics

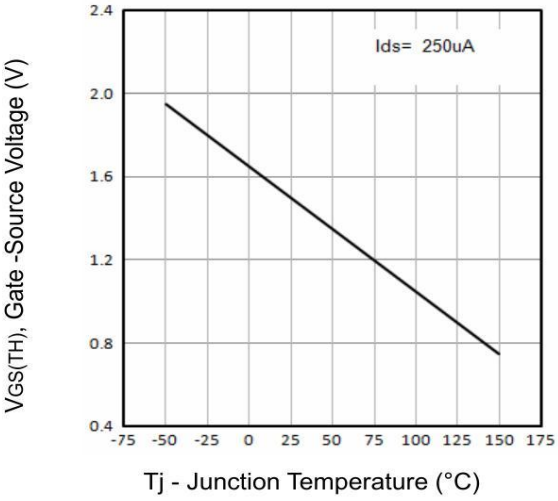


Fig2. Threshold Voltage Vs. Temperature

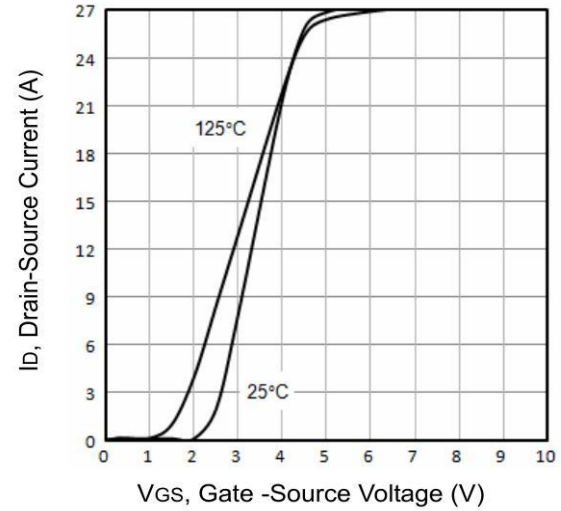


Fig3. Typical Transfer Characteristics

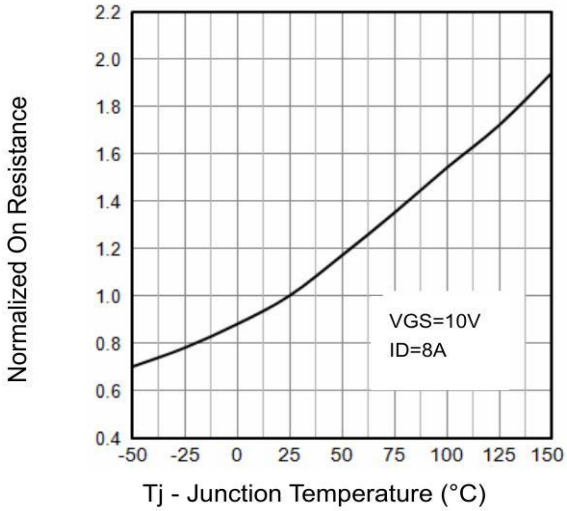


Fig4. Normalized On-Resistance Vs. Temperature

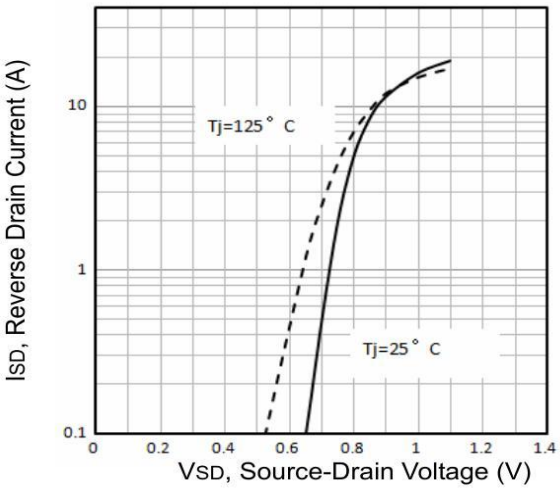


Fig5. Typical Source-Drain Diode Forward Voltage

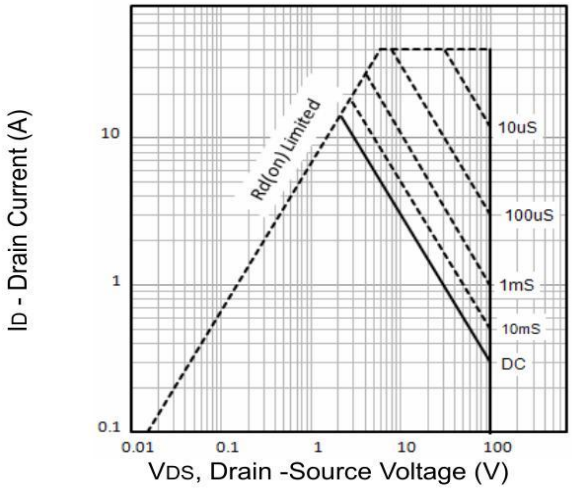


Fig6. Maximum Safe Operating Area

Electrical Characteristics Curves

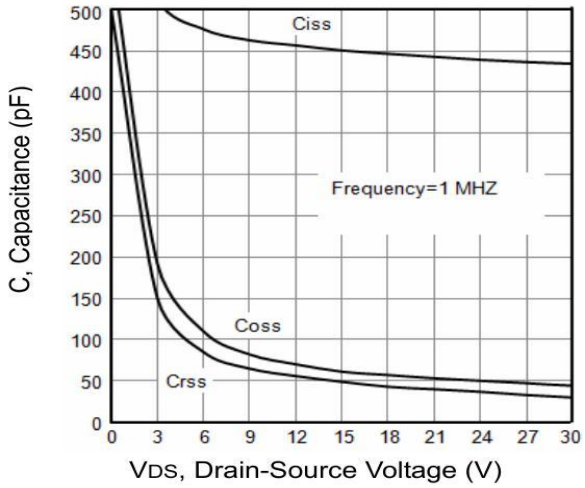


Fig7. Typical Capacitance Vs. Drain-Source Voltage

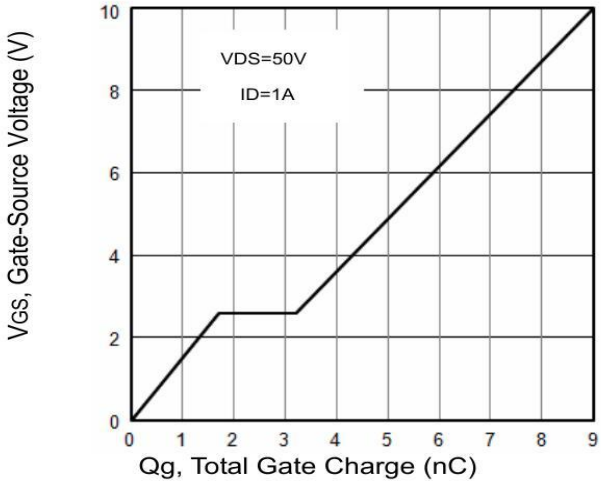


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

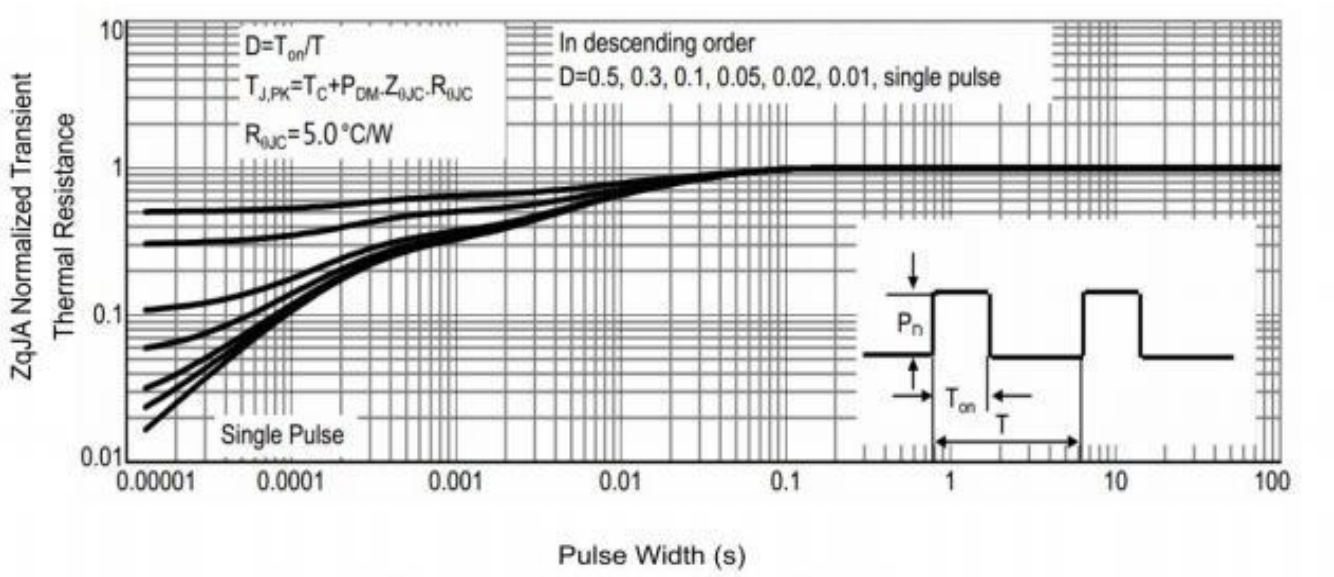


Figure 9: Normalized Maximum Transient Thermal

Test Circuits

Fig.1-1 Switching times test circuit

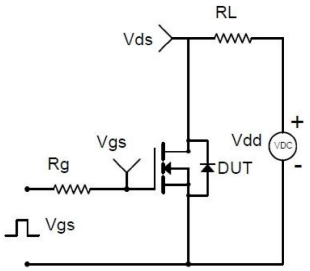


Fig.1-2 Switching Waveform

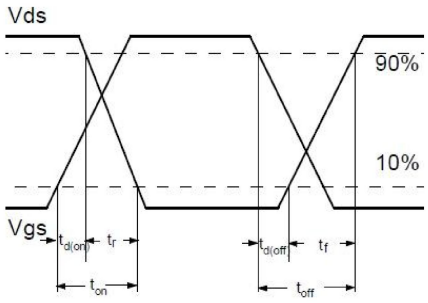


Fig.2-1 Gate charge test circuit

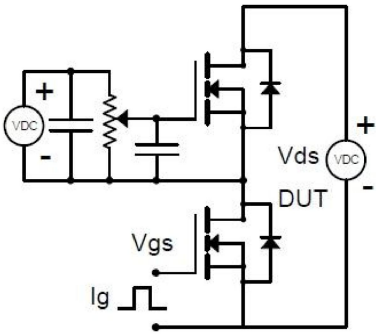


Fig.2-2 Gate charge waveform

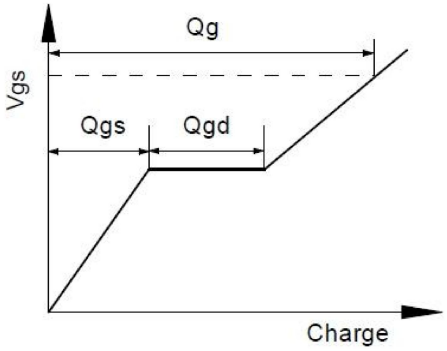


Fig.3-1 Avalanche test circuit

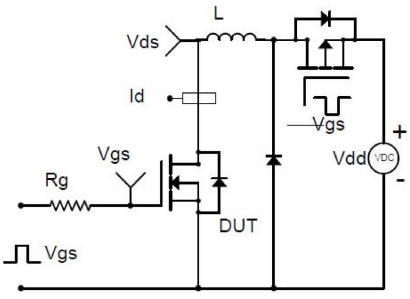
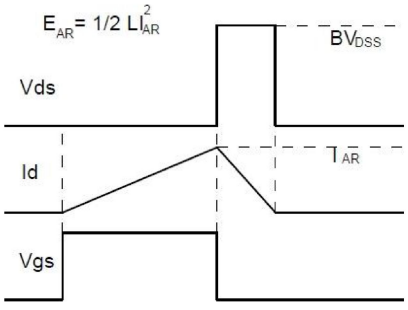
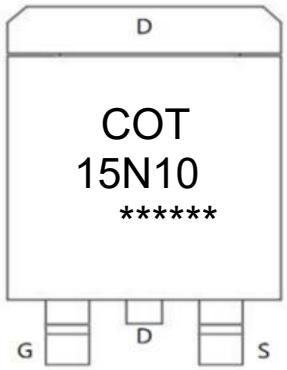


Fig.3-2 Avalanche waveform



Marking imformation



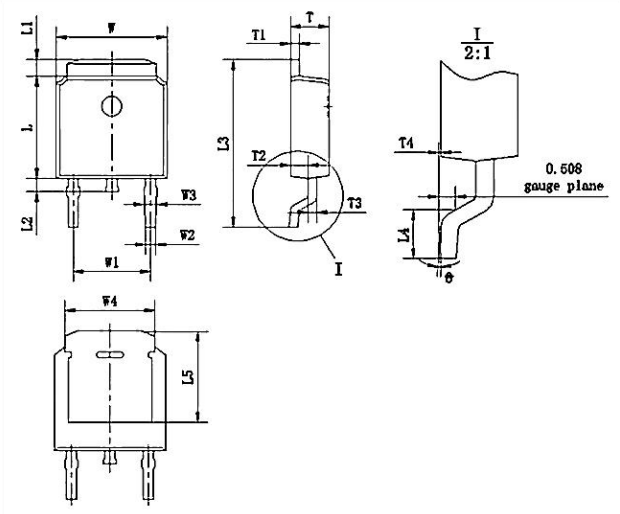
Note:

COT: Company

15N10: Product Type.

******: *: Inner Code * : Year Code **: Week Code **: Lot Code.

Package Outline Dimensions (Units: mm)



符号	尺寸		符号	尺寸		符号	尺寸	
	Min	Max		Min	Max		Min	Max
W	6.50	6.70	L1	0.8	1.2	T1	0.48	0.58
W1	(4.572)		L2	0.60	1.00	T2	0.95	1.15
W2	0.60	0.80	L3	9.70	10.30	T3	0.48	0.58
W3	0.68	0.88	L4	1.30	1.70	T4	0	0.12
W4	(5.3)		L5	(5.20)		θ	0°	8°
L	6.00	6.20	T	2.20	2.40			