

Description

This is 100V 4.5A P-Channel enhancement mode power mosfet in a SOP-8L plastic package.

Uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

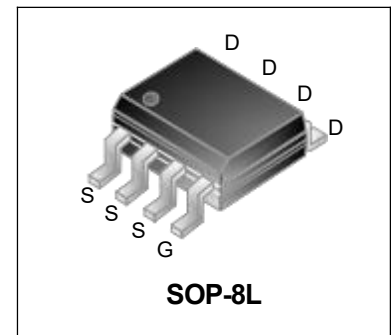
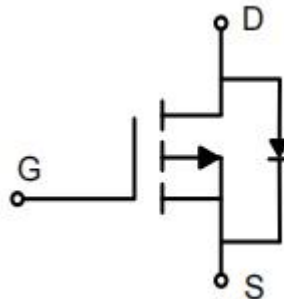
- Power Management Switches
- DC/DC converters

Features

- $V_{DS} = -100V$, $I_D = -4.5A$
 $R_{DS(on)} < 100m\Omega$ @ $V_{GS} = -10V$
 $R_{DS(on)} < 120m\Omega$ @ $V_{GS} = -4.5V$
- Extremely Low Switching Loss
- Excellent Stability and Uniformity
- Low Gate Charge
- 100% EAS Guaranteed

V_{DS}	$R_{DS(on)(typ)}$	I_D
100 V	82m Ω	4.5 A

Equivalent Circuit & Pinning



Absolute Maximum Ratings (TA = 25° C, unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	TA= 25°C	I_D	-4.5	A
	TA= 100°C		-2.8	
Pulsed Drain Current ¹		I_{DM}	-18	A
Single Pulse Avalanche Energy ²		EAS	80	mJ
Total Power Dissipation	TA= 25°C	P_D	3.1	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ³	R_{θJA}	40.3	°C/W

Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-100	-	-	V
Gate-body Leakage current		I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T _J = 25°C	I _{DSS}	V _{DS} = -100V, V _{GS} = 0V	-	-	-1	μA
	T _J = 100°C			-	-	-100	
Gate-Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1	-1.8	-2.5	V
Drain-Source On-Resistance ⁴		R _{DS(on)}	V _{GS} = -10V, I _D = -4A	-	82	100	mΩ
			V _{GS} = -4.5V, I _D = -2A		88	120	
Forward Transconductance ⁴		g _{fs}	V _{DS} = -10V, I _D = -4A	-	30	-	S
Dynamic Characteristics ⁵							
Input Capacitance		C _{iss}	V _{DS} = -50V, V _{GS} = 0V, f = 1MHz	-	4245	-	pF
Output Capacitance		C _{oss}		-	92	-	
Reverse Transfer Capacitance		C _{rss}		-	69	-	
Gate Resistance		R _g	f = 1MHz	-	4	-	Ω
Switching Characteristics ⁵							
Total Gate Charge		Q _g	V _{GS} = -10V, V _{DS} = -50V, I _D = -4A	-	65	-	nC
Gate-Source Charge		Q _{gs}		-	10.2	-	
Gate-Drain Charge		Q _{gd}		-	13	-	
Turn-On Delay Time		t _{d(on)}	V _{GS} = -10V, V _{DD} = -50V, R _G = 3Ω, I _D = -4A	-	12.8	-	ns
Rise Time		t _r		-	30	-	
Turn-Off Delay Time		t _{d(off)}		-	82	-	
Fall Time		t _f		-	61	-	
Body Diode Reverse Recovery Time		t _{rr}	I _F = -4A, dI/dt= 100A/μs	-	62	-	ns
Body Diode Reverse Recovery Charge		Q _{rr}		-	56	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴		V _{SD}	I _S = -4A, V _{GS} = 0V	-	-	-1.2	V
Continuous Source Current	T _A = 25°C	I _S	-	-	-	-4.5	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature T_J(MAX)=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.4mH, I_{AS}= -20A
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test..

Typical Characteristic

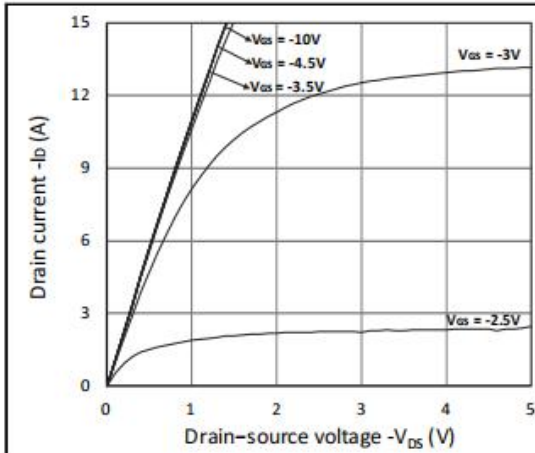


Figure 1. Output Characteristics

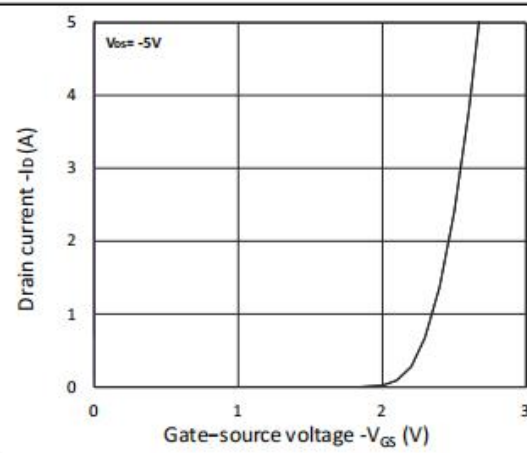


Figure 2. Transfer Characteristics

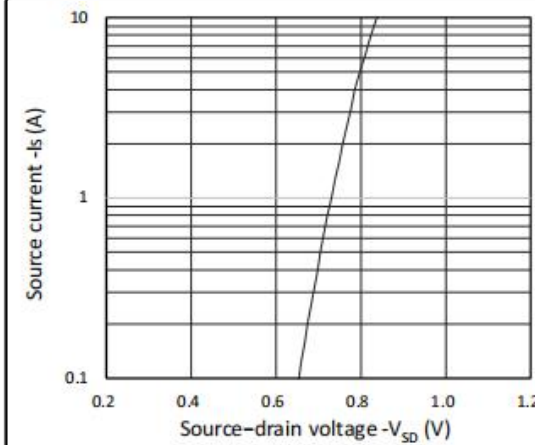


Figure 3. Forward Characteristics of Reverse

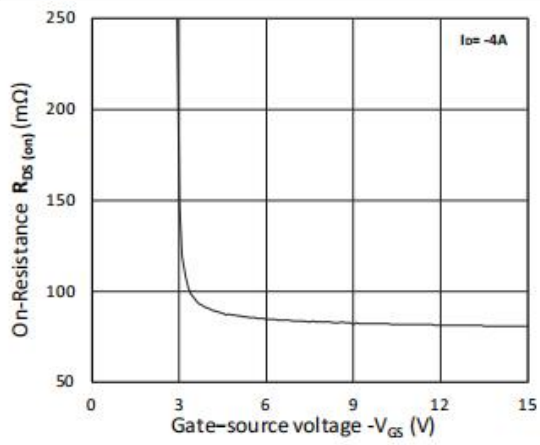


Figure 4. $R_{DS(on)}$ vs. V_{GS}

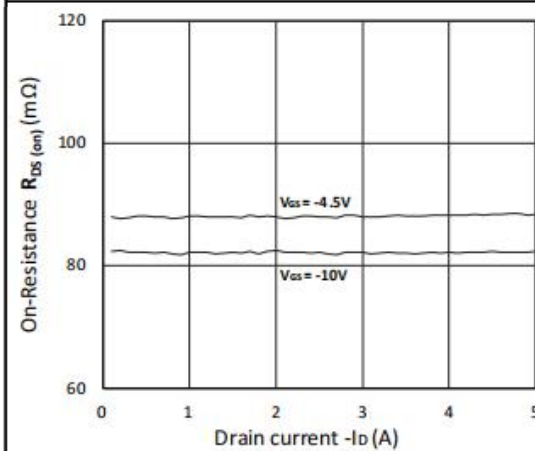


Figure 5. $R_{DS(on)}$ vs. I_D

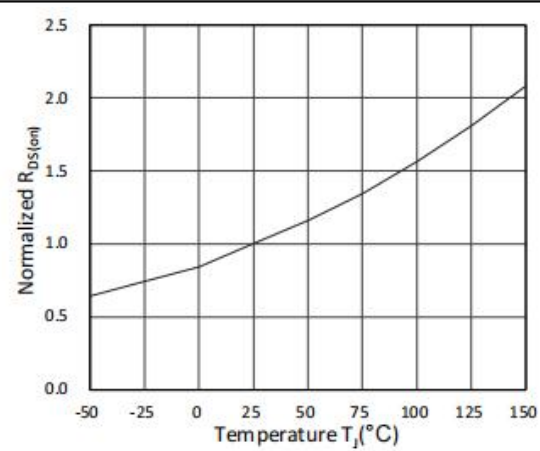


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

Typical Characteristic

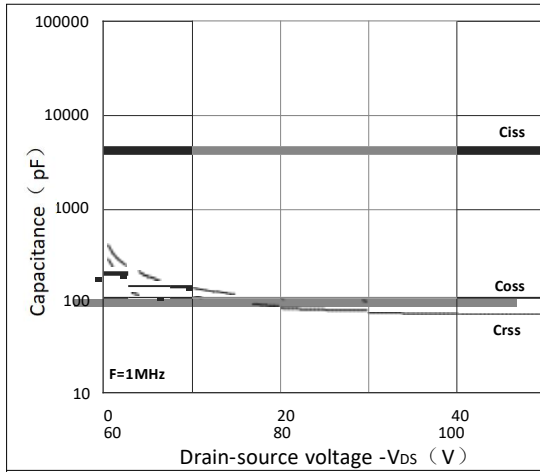


Figure 7. Capacitance Characteristics

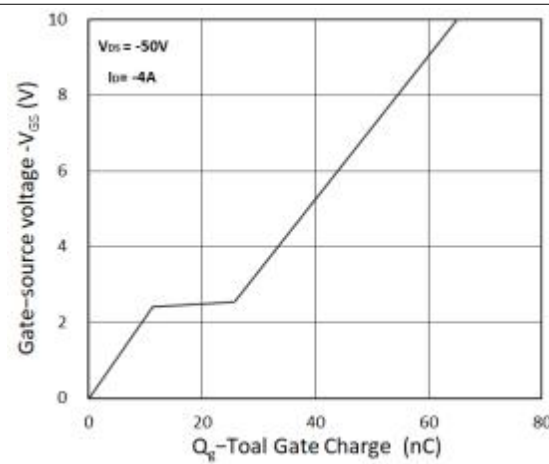


Figure 8. Gate Charge Characteristics

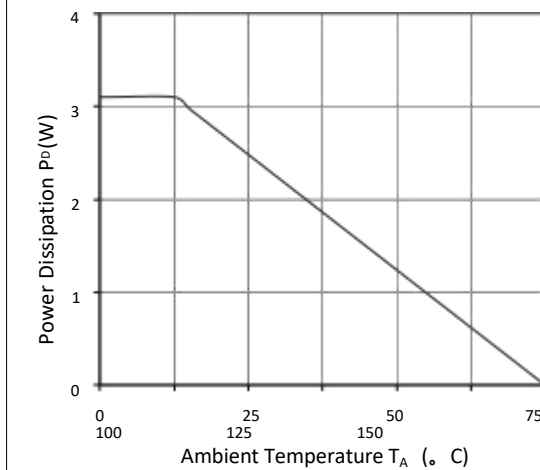


Figure 9. Power Dissipation

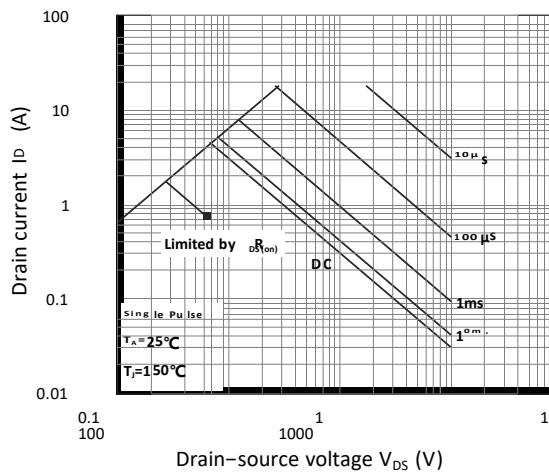


Figure 10. Safe Operating Area

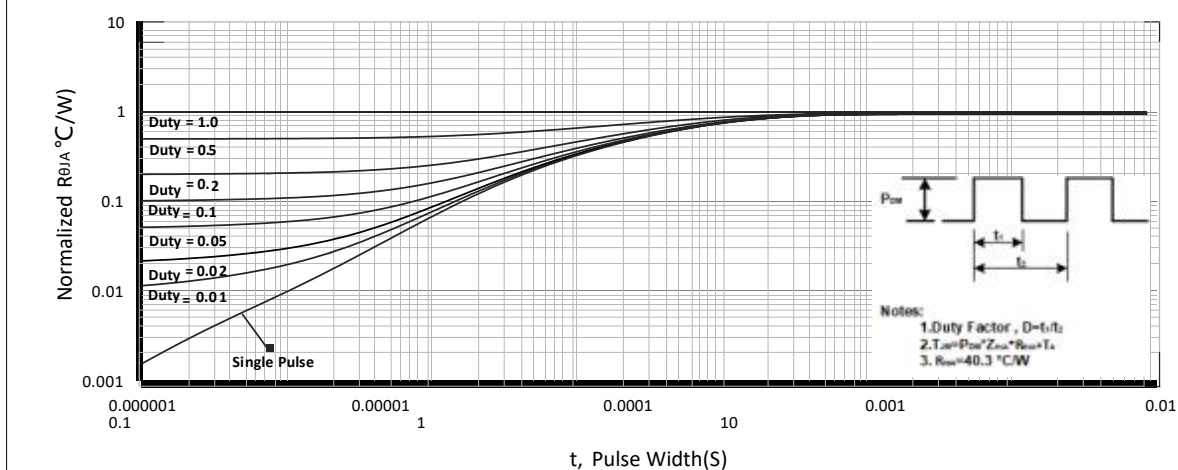


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

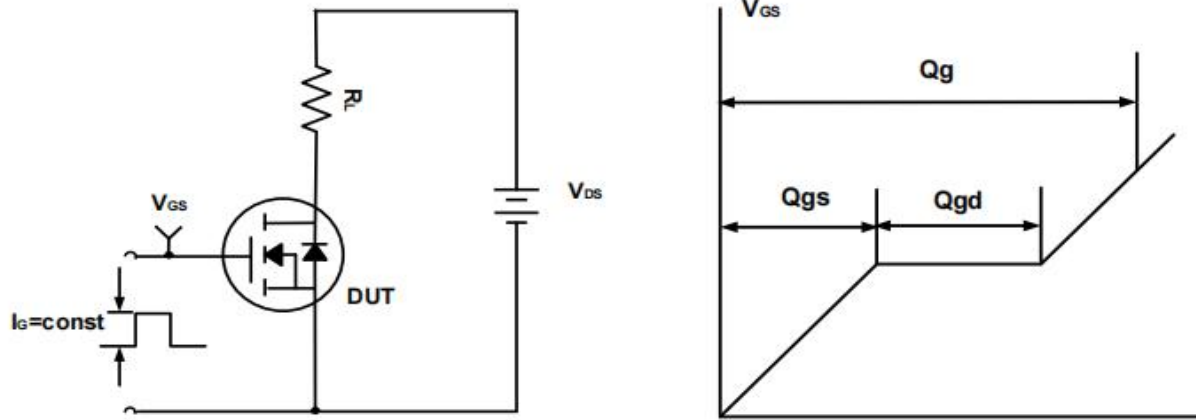


Figure A. Gate Charge Test Circuit & Waveforms

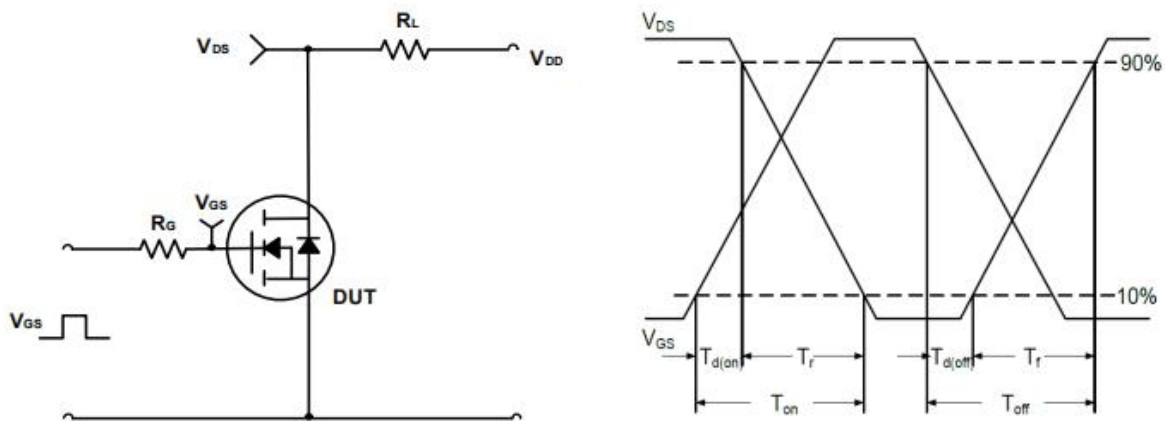


Figure B. Switching Test Circuit & Waveforms

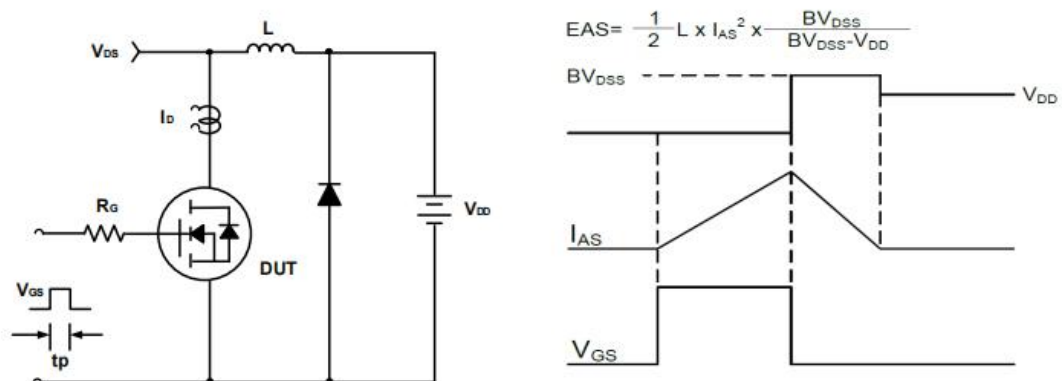
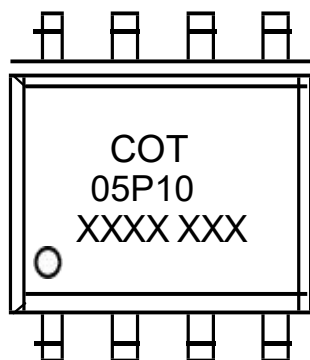


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Marking Information



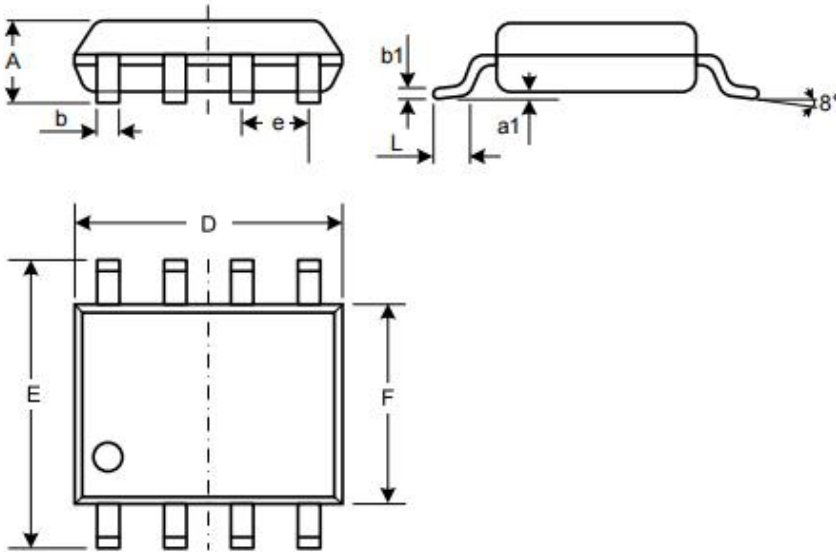
05P10= Device code

XXXX XXX= Date code

Ordering Information

Part	Package	Marking	Packing method
CT05P10SA	SOP-8L	05P10	Tape and Reel

Mechanical Dimensions for SOP-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	1.35	1.75
a1	0.05	0.25
b	0.31	0.51
b1	0.16	0.25
D	4.70	5.15
E	5.75	6.25
e	1.07	1.47
F	3.70	4.10
L	0.40	1.27