Description

This is CT50P03ZT uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Mechanical Characteristics

- Power Management Switches
- Battery Protection Application

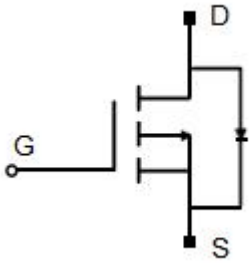
Features

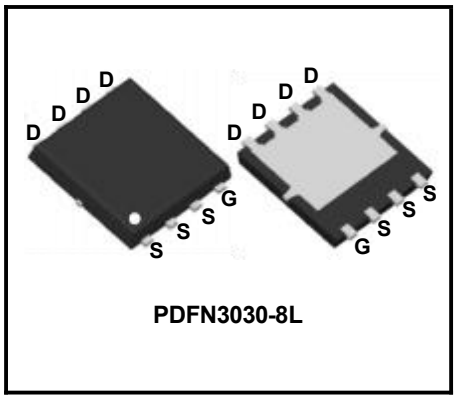
- VDS= -30V, ID = -50A
  RDS(on) < 9mΩ @ VGS = - 10V
  RDS(on) < 14mΩ @ VGS = -4.5V
- Green Device Available
- Low Gate Charge
- Advanced High Cell Density Trench Technology
- 100% EAS Guaranteed

V_{DSS}	$R_{DS(on)}$ (typ)	I_D
-30 V	5.8mΩ	-50 A

Equivalent Circuit & Pinning

RoHS compliant





PDFN3030-8L

Absolute Maximum Ratings(Ta=25℃)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	Tc=25°C	I_D	-50	A
	Tc=100°C		-32	
Pulsed Drain Current[1]		I_{DM}	-200	A
Single Pulse Avalanche Energy[2]		EAS	80	mJ
Total Power Dissipation	Tc=25°C	P_D	69	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Absolute Maximum Ratings(Ta=25℃)

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[3]	$R_{\theta JA}$	65	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.8	°C/W

Electrical Characteristics(Ta=25℃)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30	-	-	V
Gate-body Leakage current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25°C	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V	-	-	-1	μA
	T_J=100°C			-	-	-100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-	-2.5	V
Drain-Source On-Resistance[4]		$R_{DS(on)}$	V_{GS} = -10V, I_D = -20A	-	5.8	9	mΩ
			V_{GS} = -4.5V, I_D = -15A	-	8	14	
Forward Transconductance[4]		g_{fs}	V_{DS} = -10V, I_D = -20A	-	50	-	S
Dynamic Characteristics[5]							
Input Capacitance		C_{iss}	V_{DS} = -15V, V_{GS} =0V, f =1MHz	-	3520	-	pF
Output Capacitance		C_{oss}		-	465	-	
Reverse Transfer Capacitance		C_{rss}		-	370	-	
Gate Resistance		R_g	f=1MHz	-	9.5	-	Ω
Switching Characteristics[5]							
Total Gate Charge		Q_g	V_{GS} = -10V,V_{DS} = -15V, I_D= -20A	-	35	-	nC
Gate-Source Charge		Q_{gs}		-	9.9	-	
Gate-Drain Charge		Q_{gd}		-	10.5	-	
Turn-On Delay Time		$t_{d(on)}$	V_{GS} = -10V, V_{DD} = -15V, R_G = 3Ω, I_D= -20A	-	10.8	-	ns
Rise Time		t_r		-	13.2	-	
Turn-Off Delay Time		$t_{d(off)}$		-	73	-	
Fall Time		t_f		-	35	-	
Body Diode Reverse Recovery Time		t_{rr}	I_F = -20A, dI/dt = 100A/μs	-	25	-	ns
Body Diode Reverse Recovery Charge		Q_{rr}		-	10	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		V_{SD}	I_S = -1A, V_{GS} = 0V	-	-	-1.2	V
Continuous Source Current	T_C=25°C	I_S	-	-	-	-50	A

Note :

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.1mH, I_{AS}= -40A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test..

Typical Characteristics

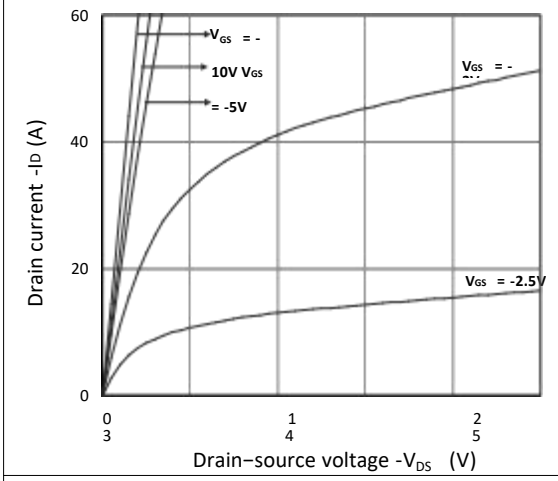


Figure 1. Output Characteristics

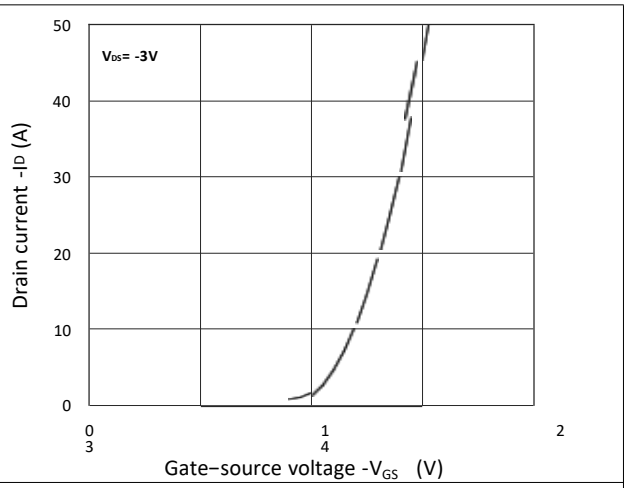


Figure 2. Transfer Characteristics

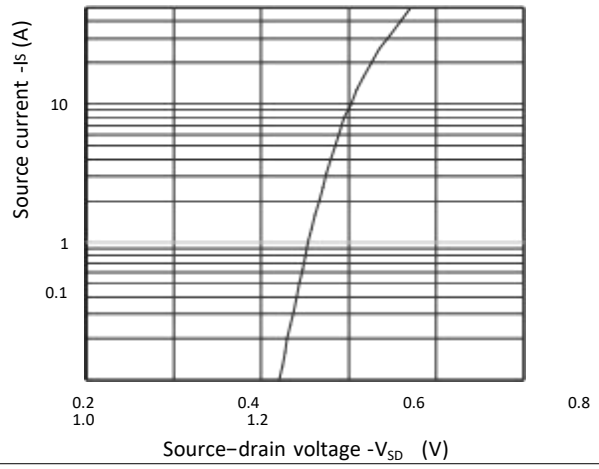


Figure 3. Forward Characteristics of Reverse

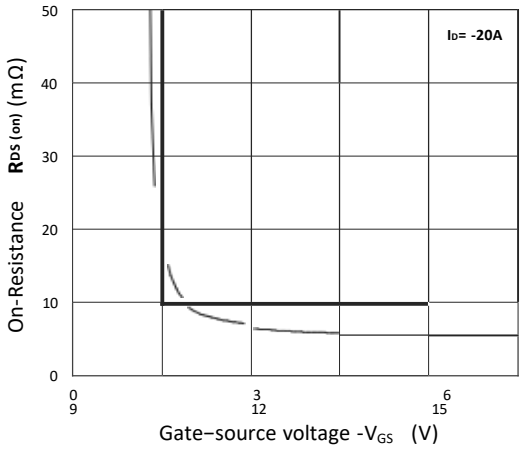


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

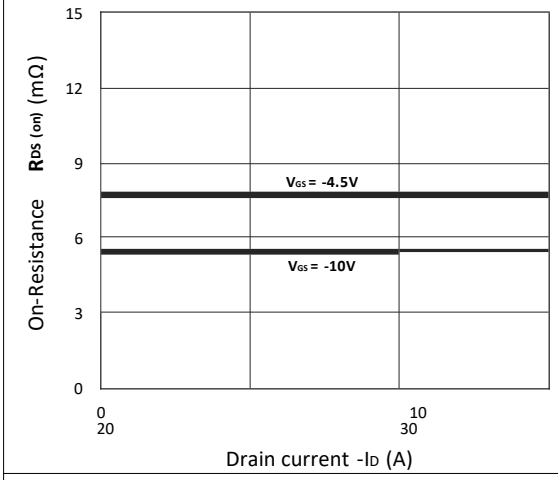


Figure 5. $R_{DS(ON)}$ vs. I_D

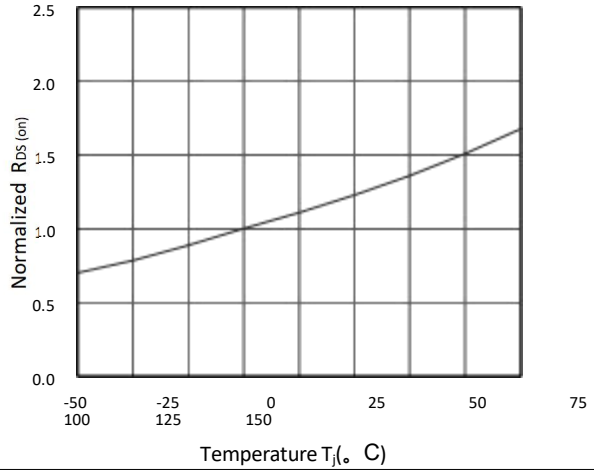


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

Typical Characteristics

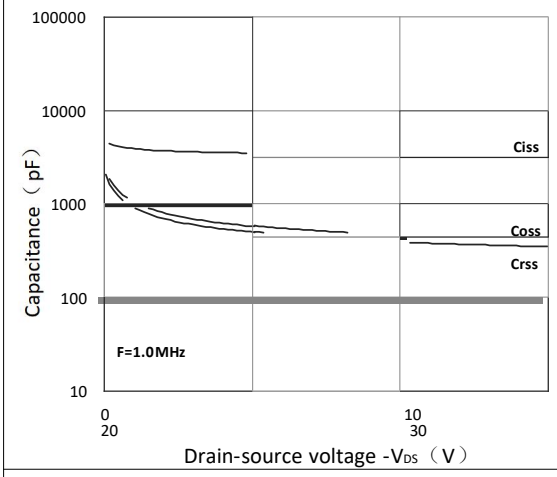


Figure 7. Capacitance Characteristics

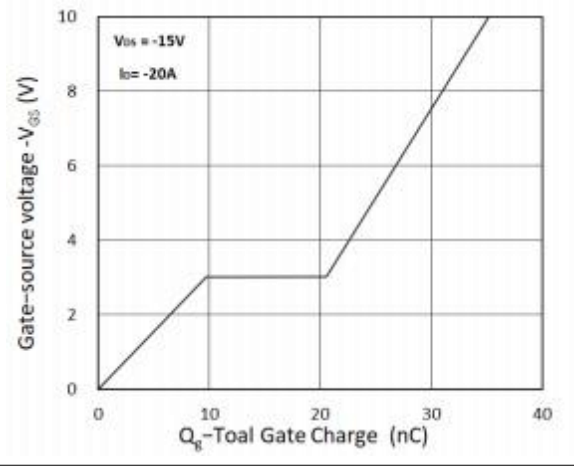


Figure 8. Gate Charge Characteristics

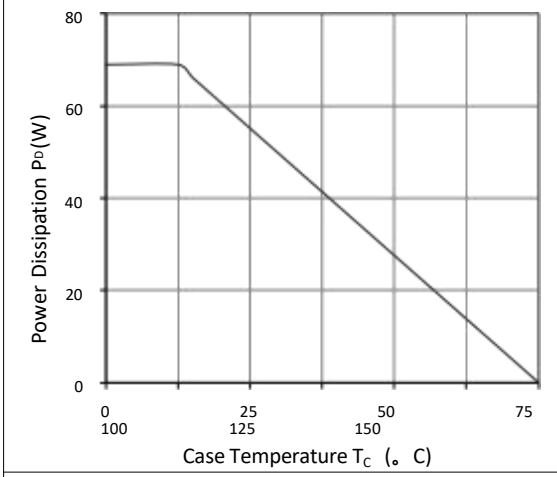


Figure 9. Power Dissipation

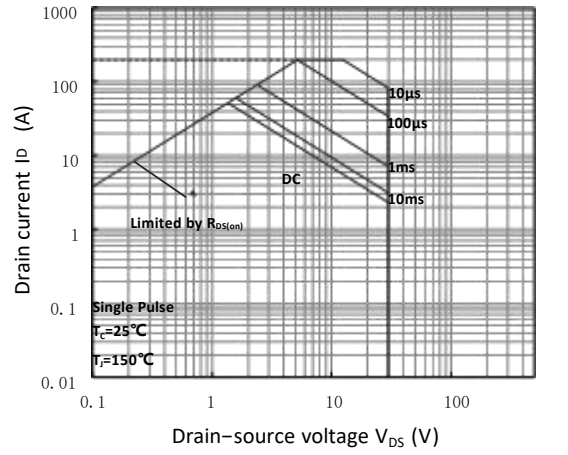


Figure10. Safe Operating Area

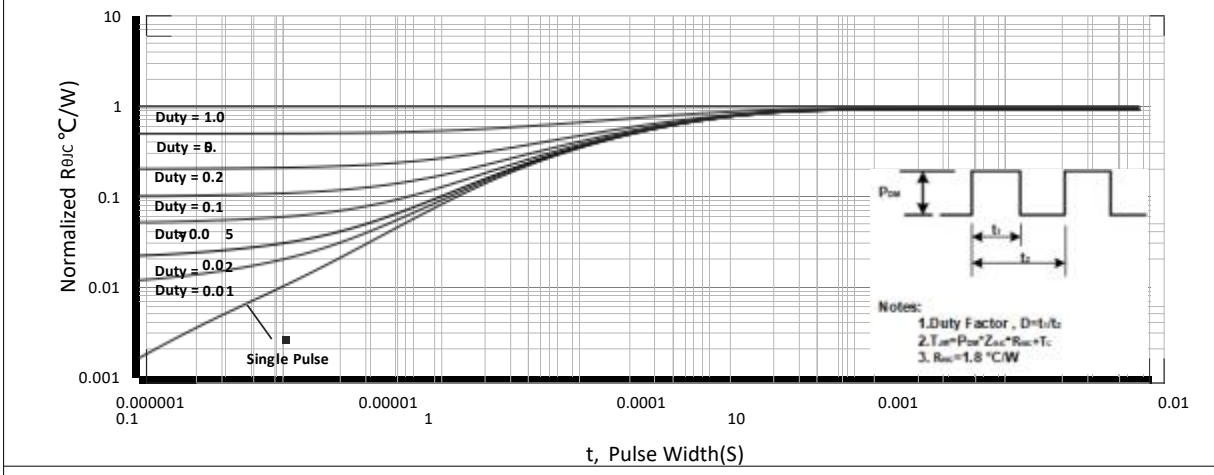


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

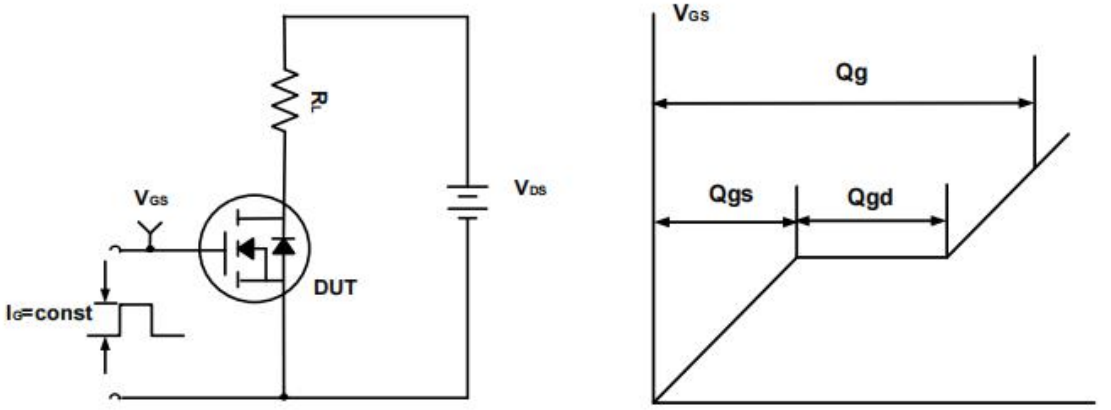


Figure A. Gate Charge Test Circuit & Waveforms

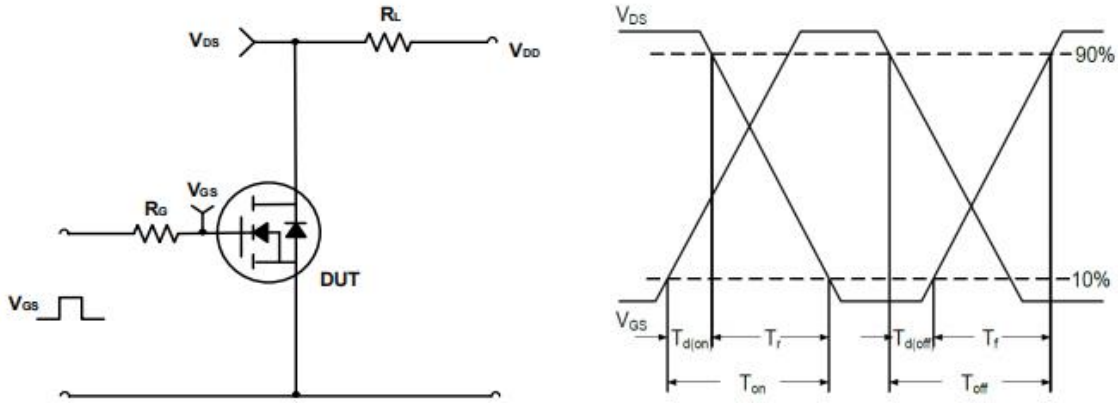


Figure B. Switching Test Circuit & Waveforms

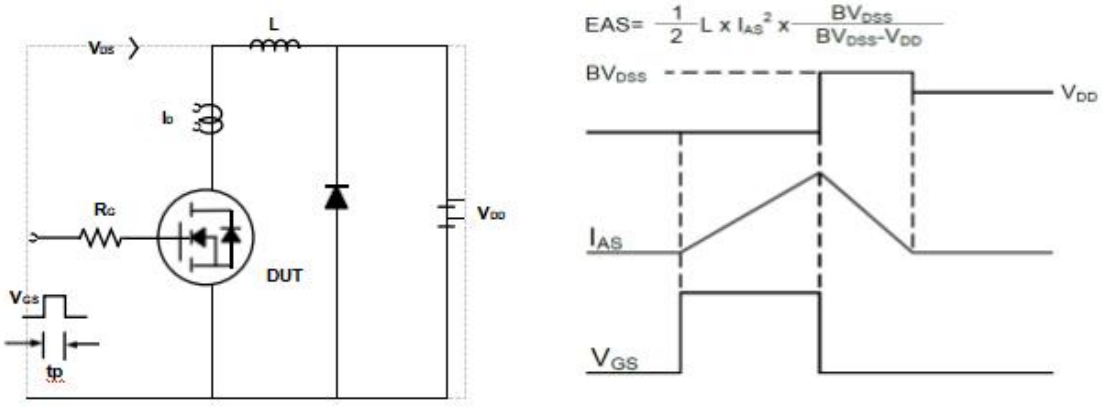
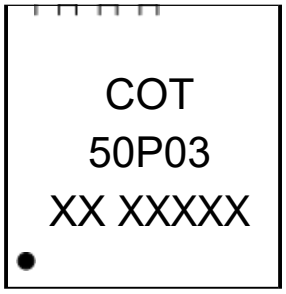


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Marking Codes

Part	Package	Marking	Packing method
CT50P03ZT	PDFN3030-8L	50P03	Tape and Reel

Marking Information

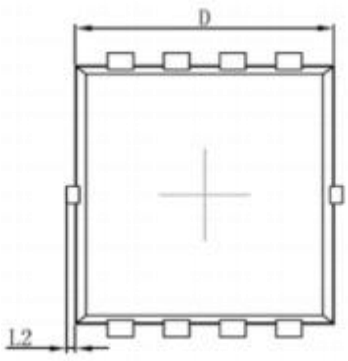


COT= Company Logo

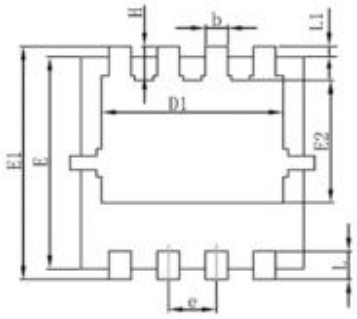
50P03= Device code

XX XXXXX= Date code

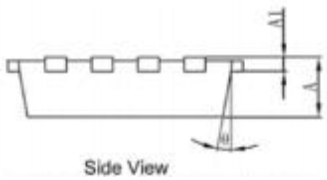
Mechanical Dimensions for PDFN3030-8L



Topview



Botomvew



Side View

COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	0.65	0.90
A1	0.10	0.25
D	2.90	3.25
D1	2.25	2.69
E	2.90	3.20
E1	3.00	3.60
E2	1.35	2.20
b	0.20	0.40
e	0.65BSC	
L	0.15	0.50
L1	0.13BSC	
L2	0.00	0.20
H	0.15	0.65
θ	0°	14°