Description

This is 100V 95A N-channel mosfet in a PDFN5060-8L plastic package.

Uses generation power trench MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications.

Features

- VDS= 100V, ID = 95A

  RDS(on) < 6mΩ @ VGS = 10V

  RDS(on) < 9mΩ @ VGS = 4.5V
- Green Device Available
- Low Gate Charge
- 100% EAS Guaranteed

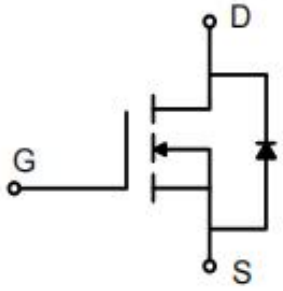
Applications

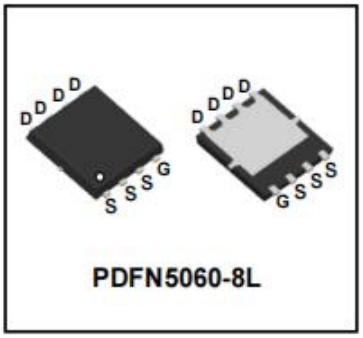
- Power management switches
- DC/DC converter
- LED Backlighting

V_{DSS}	$R_{DS(on)TYP}$	I_D
100 V	4.5mΩ	95 A

Equivalent Circuit & Pinning

RoHS compliant





Absolute Maximum Ratings(Ta=25℃)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	95	A
	T_C=100°C		60	
Pulsed Drain Current[4]		I_{DM}	380	A
Single Pulse Avalanche Energy[3]		EAS	205	mJ
Total Power Dissipation	T_C=25°C	P_D	113.6	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[1]	$R_{\theta JA}$	58	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.1	°C/W

Electrical Characteristics (Ta=25℃)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	-	-	V
Gate-body Leakage current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25°C	I_{DSS}	V_{DS} =100V, V_{GS} = 0V	-	-	1	μA
	T_J=100°C			-	-	100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.8	2.5	V
Drain-Source on-Resistance[2]		$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	4.5	6	mΩ
			V_{GS} = 4.5V, I_D = 15A	-	6.6	9	
Dynamic Characteristics							
Input Capacitance		C_{iss}	V_{DS} = 50V, V_{GS} =0V, f =1MHz	-	4400	-	pF
Output Capacitance		C_{oss}		-	645	-	
Reverse Transfer Capacitance		C_{rss}		-	20	-	
Switching Characteristics							
Gate Resistance		R_g	V_{GS} = 0V, V_{DS} = 0V, f =1MHz	-	1.7	-	Ω
Total Gate Charge		Q_g	V_{GS} = 10V, V_{DS} = 50V, I_D=20A	-	75	-	nC
Gate-Source Charge		Q_{gs}		-	17	-	
Gate-Drain Charge		Q_{gd}		-	13	-	
Turn-on Delay Time		$t_{d(on)}$	V_{GS} =10V, V_{DS} =50V, R_G = 3Ω, I_D= 20A	-	15.4	-	ns
Rise Time		t_r		-	13	-	
Turn-off Delay Time		$t_{d(off)}$		-	34	-	
Fall Time		t_f		-	6.2	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[2]		V_{SD}	I_F = 20A, V_{GS} = 0V	-	-	1.2	V
Continuous Source Current[1,5]		I_S	V_G=V_D=0V , Force Current	-	-	95	A
Body Diode Reverse Recovery Time		t_{rr}	I_F = 20A, dI/dt=100A/μs	-	55	-	ns
Body Diode Reverse Recovery Charge		Q_{rr}		-	101	-	nC

Notes:

1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
3. The EAS data shows Max. rating . The test condition is V_{DD}=50V, V_{GS}=10V, L=0.4mH, I_{AS}=32A
4. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Electrical Characteristic Curve

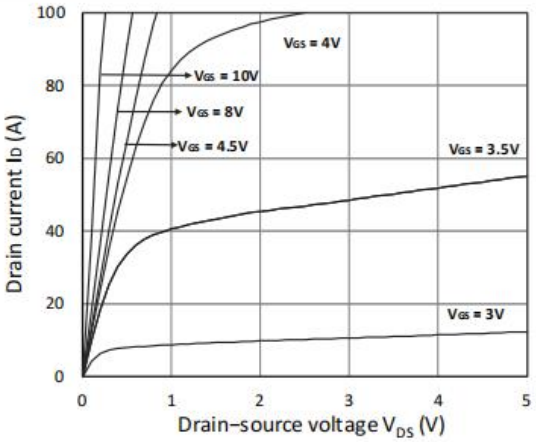


Figure 1. Output Characteristics

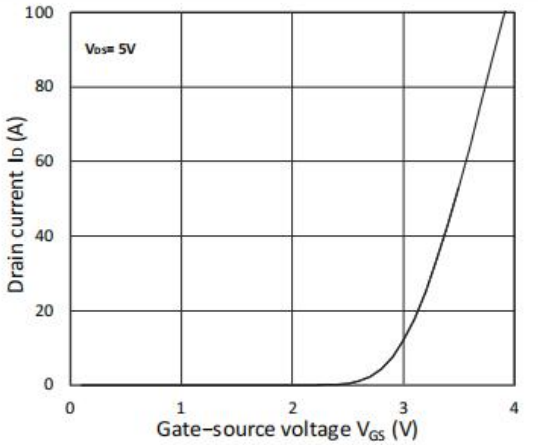


Figure 2. Transfer Characteristics

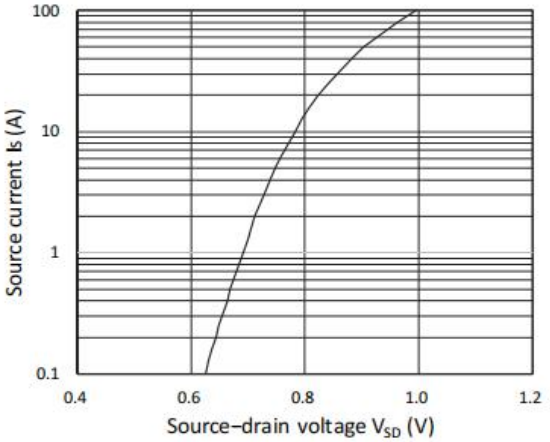


Figure 3. Forward Characteristics of Reverse

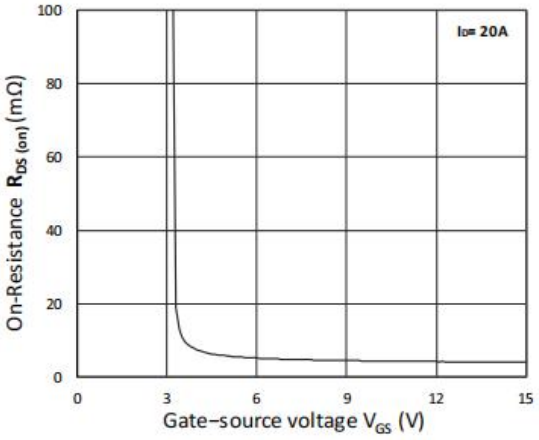


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

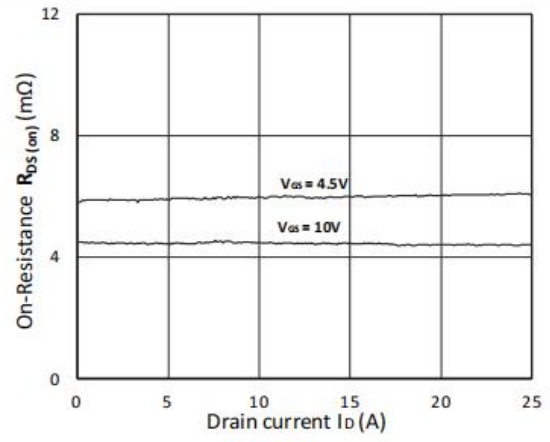


Figure 5. $R_{DS(ON)}$ vs. I_D

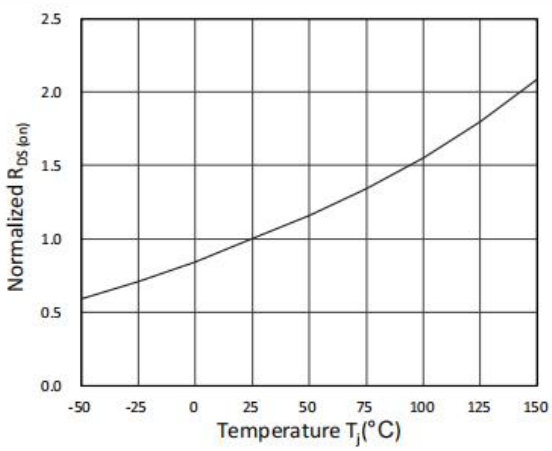


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

Electrical Characteristic Curve

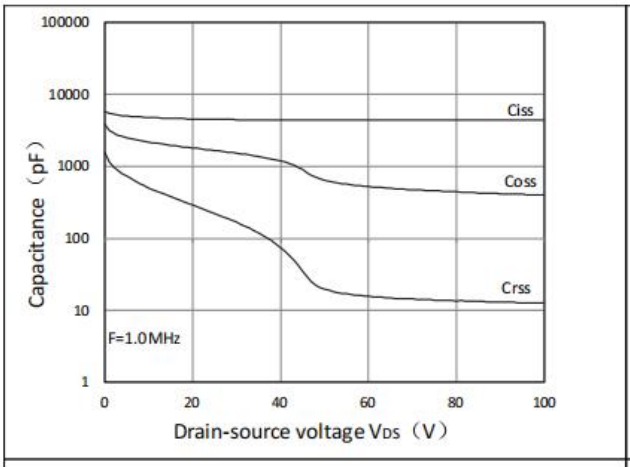


Figure 7. Capacitance Characteristics

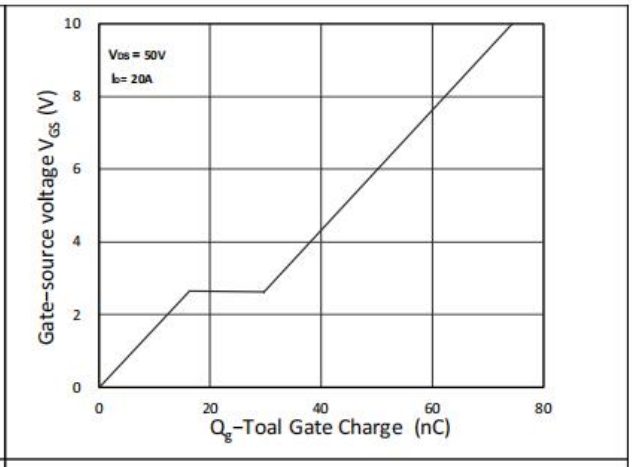


Figure 8. Gate Charge Characteristics

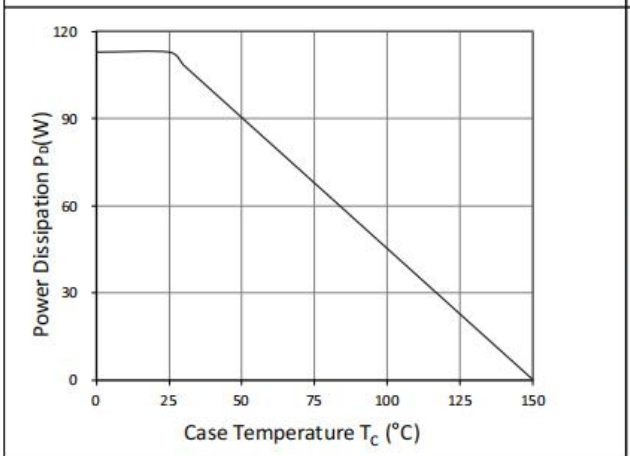


Figure 9. Power Dissipation

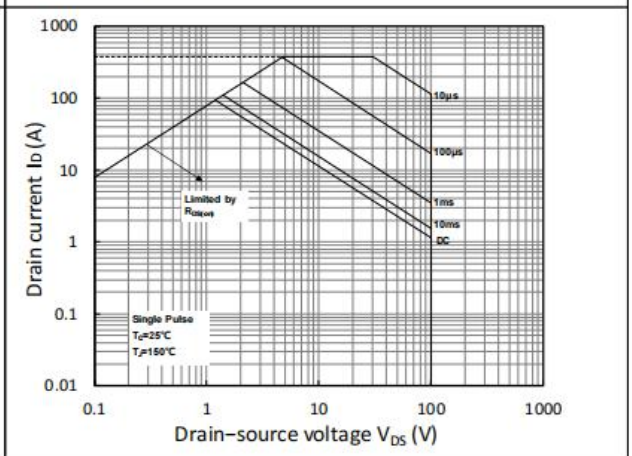


Figure10. Safe Operating Area

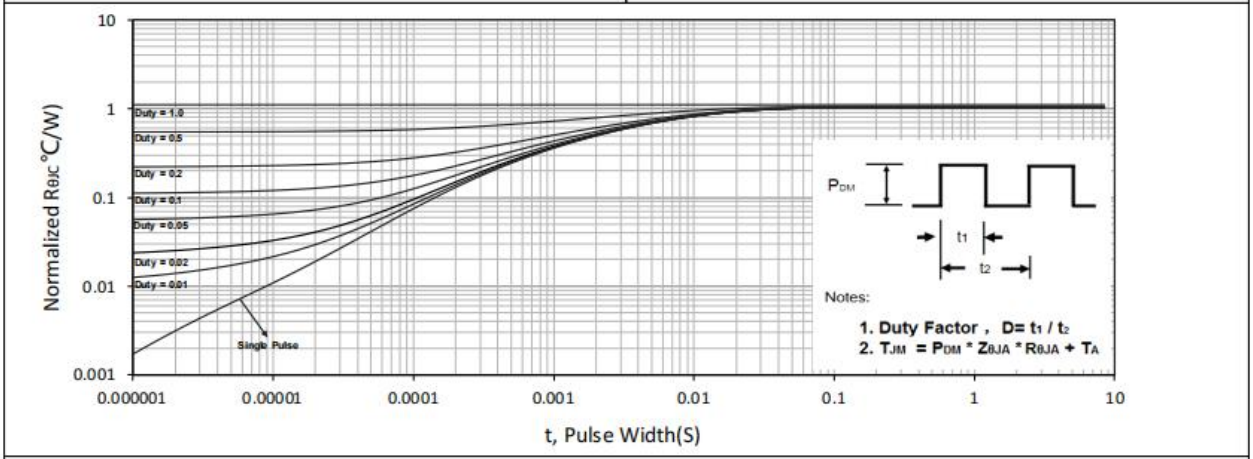


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

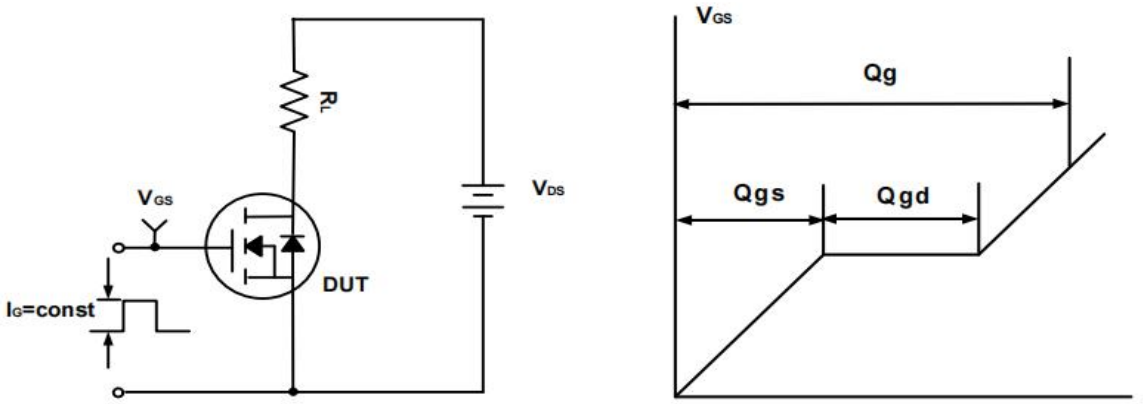


Figure A. Gate Charge Test Circuit & Waveforms

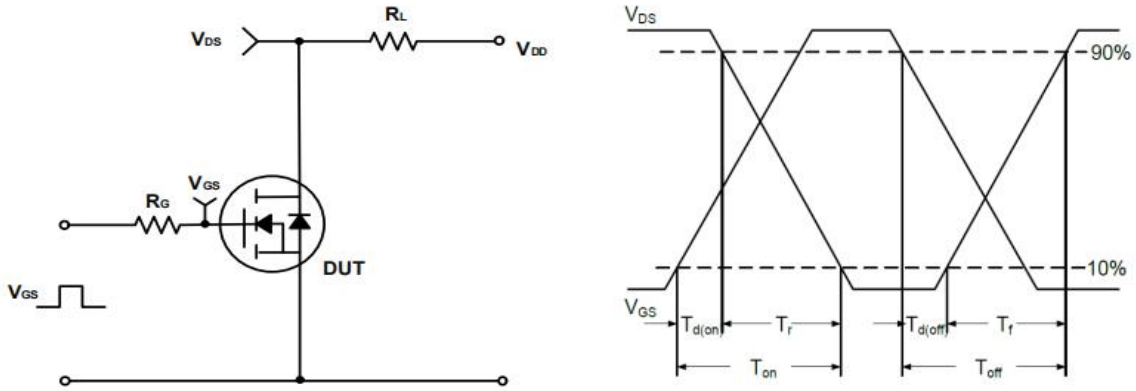


Figure B. Switching Test Circuit & Waveforms

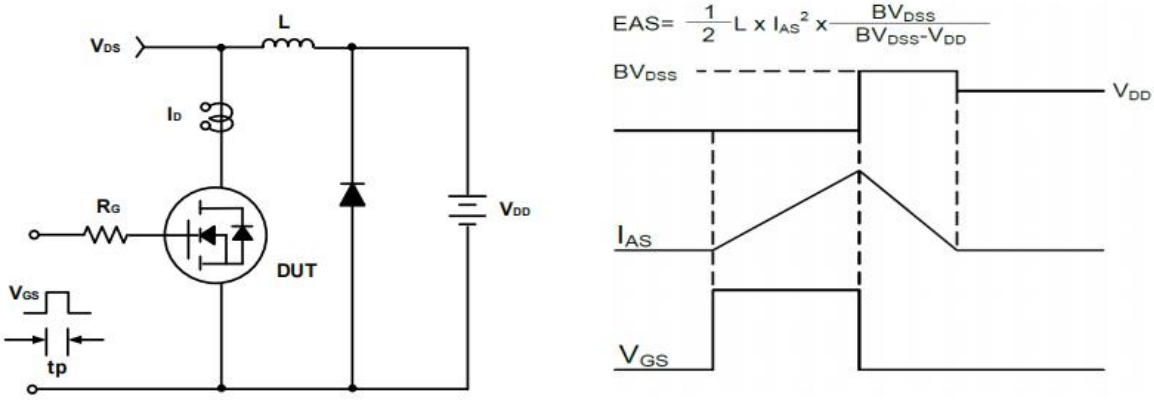
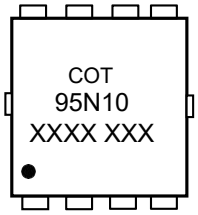


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Marking Instructions



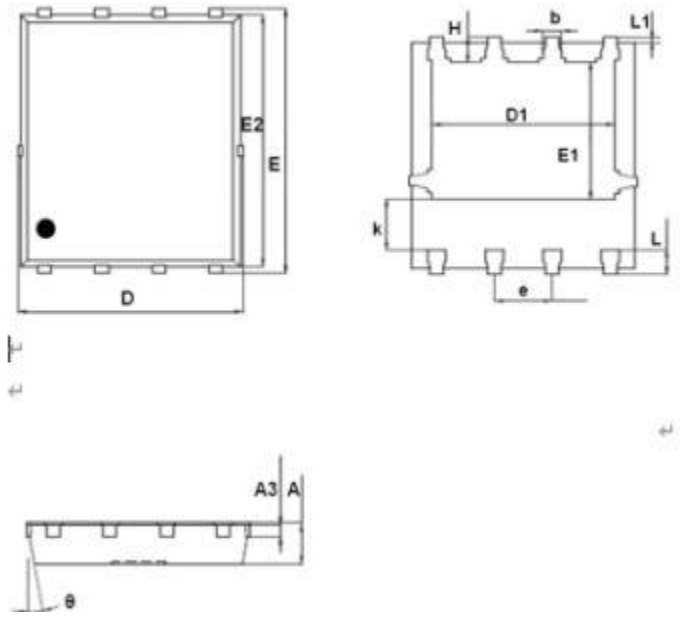
95N10 = Device code

XXXX XXX= Date code

Ordering Information

Part	Package	Marking	Packing method
CT95N10ZC	PDFN5060-8L	95N10	Tape and Reel

Mechanical Dimensions for PDFN5060-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	0.9	1.2
A3	0.15	0.35
D	4.8	5.4
E	5.9	6.35
D1	3.61	4.31
E1	3.3	3.92
E2	5.5	6.06
k	1.1	-
b	0.3	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.71
θ	0。	12。