Description

This is 65V 96A N-Channel enhancement mode power mosfet in a PDFN5060-8L plastic package.

Generation power trench mosfet technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications

Applications

- Synchronous Rectification
- DC/DC Converter

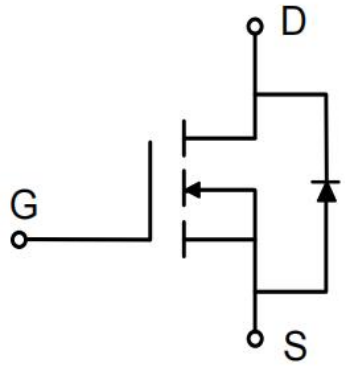
V_{DS}(V)	I_D(A)	$RDS_{(on)}$Max (mΩ)
65	96	4.8@VGS = 10V
		6.6@VGS= 4.5V

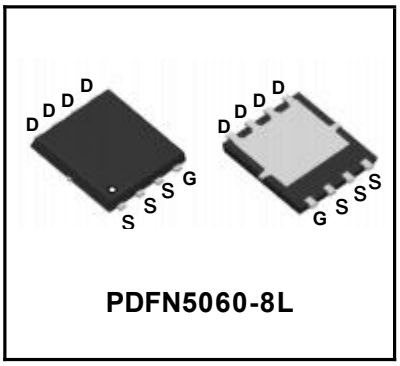
Features

- Low RDS(ON)
- 100% EAS Guaranteed
- High Speed Power Switching

Equivalent Circuit & Pinning

RoHS compliant





PDFN5060-8L

Absolute Maximum Ratings(Ta=25℃)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		**VDS**	65	V
Gate-Source Voltage		**VGS**	±20	V
Continuous Drain Current	TC=25°C	**ID**	96	A
	TC=100°C		61	
Pulsed Drain Current[1]		**IDM**	380	A
Single Pulse Avalanche Energy[2]		**EAS**	182.25	mJ
Total Power Dissipation	TC=25°C	**PD**	73.5	W
Operating Junction and Storage Temperature Range		**TJ , TSTG**	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[3]	**RθJA**	51	°C/W
Thermal Resistance from Junction-to-Case	**RθJC**	1.7	°C/W

Electrical Characteristics(Ta=25℃)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		**V(BR)DSS**	VGS = 0V, ID = 250μA	65	-	-	V
Gate-body Leakage Current		**IGSS**	VDS = 0V, VGS = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	TJ=25°C	**IDSS**	VDS = 65V, VGS = 0V	-	-	1	μA
	TJ=100°C			-	-	100	
Gate-Threshold Voltage		**VGS(th)**	VDS = VGS, ID = 250μA	1.2	1.7	2.5	V
Drain-Source On-Resistance[4]		**RDS(on)**	VGS = 10V, ID = 20A	-	3.5	4.8	mΩ
			VGS = 4.5V, ID = 10A	-	4.8	6.6	
Forward Transconductance[4]		**gfs**	VDS = 10V, ID = 20A	-	89	-	S
Dynamic Characteristics[5]							
Input Capacitance		**Ciss**	VDS = 30V, VGS =0V, f =1MHz	-	2180	-	pF
Output Capacitance		**Coss**		-	735	-	
Reverse Transfer Capacitance		**Crss**		-	42	-	
Gate Resistance		**Rg**	f = 1MHz	-	1.8	-	Ω
Switching Characteristics[5]							
Total Gate Charge		**Qg**	VGS = 10V, VDS = 30V, ID= 20A	-	35	-	nC
Gate-Source Charge		**Qgs**		-	6.6	-	
Gate-Drain Charge		**Qgd**		-	8.4	-	
Turn-On Delay Time		**td(on)**	VGS =10V, VDD = 30V, RG = 3Ω, ID= 20A	-	9.4	-	ns
Rise Time		**tr**		-	8.4	-	
Turn-Off Delay Time		**td(off)**		-	32.5	-	
Fall Time		**tf**		-	12.5	-	
Body Diode Reverse Recovery Time		**trr**	IF=20A, dI/dt=100A/μs	-	50	-	ns
Body Diode Reverse Recovery Charge		**Qrr**		-	20	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		**VSD**	IS = 20A, VGS = 0V	-	-	1.2	V
Continuous Source Current	TC=25°C	**IS**	-	-	-	96	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature TJ(MAX)=150°C
2. The EAS data shows Max. rating . The test condition is VDD=25V,VGS=10V,L=0.5mH，IAS=27A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test

Typical Characteristics

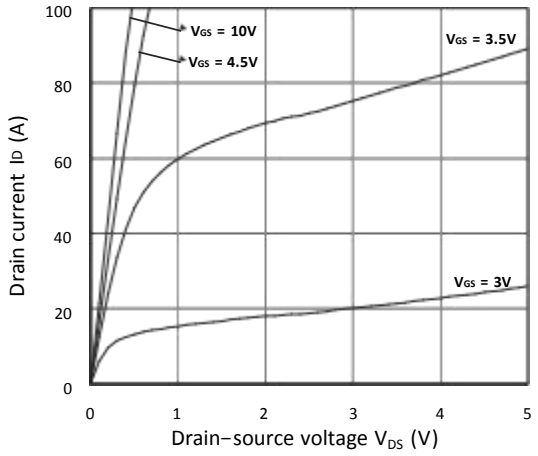


Figure 1. Output Characteristics

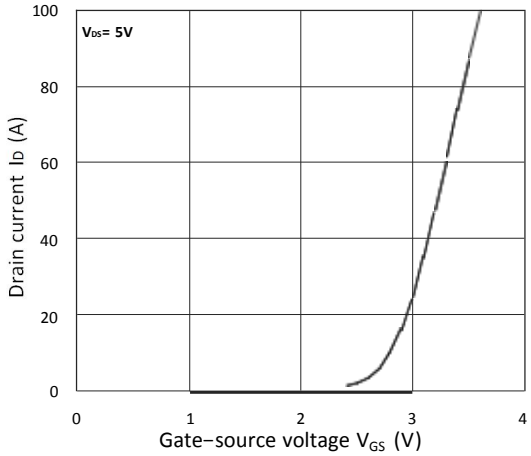


Figure 2. Transfer Characteristics

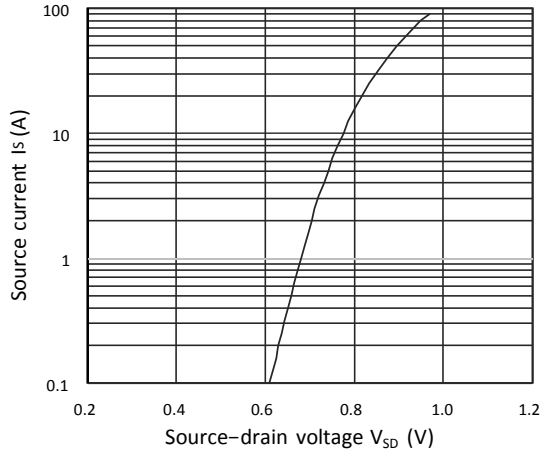


Figure 3. Forward Characteristics of Reverse

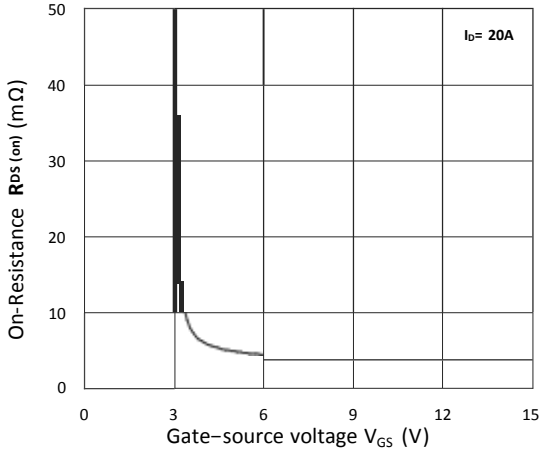


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

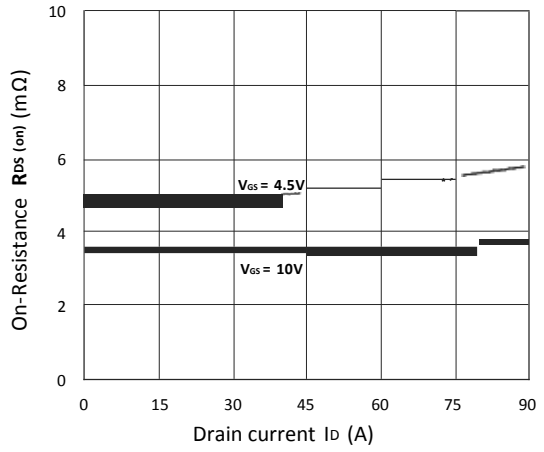


Figure 5. $R_{DS(ON)}$ vs. I_D

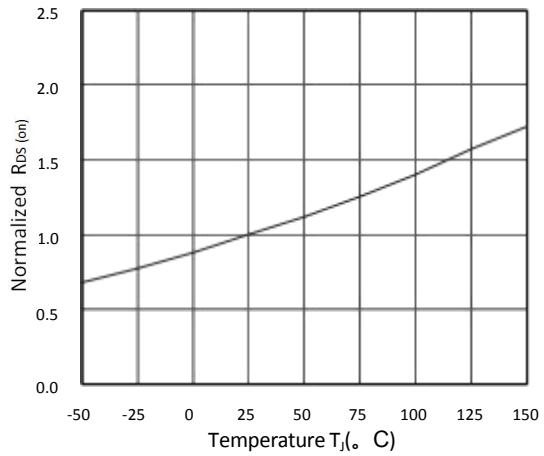


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

Typical Characteristics

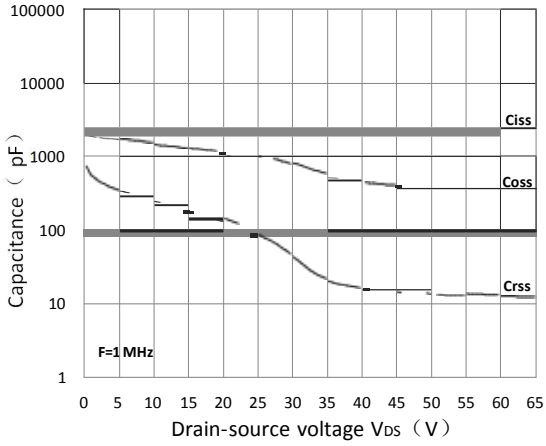


Figure 7. Capacitance Characteristics

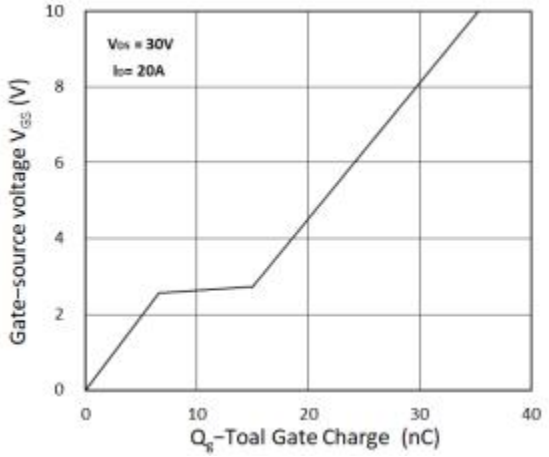


Figure 8. Gate Charge Characteristics

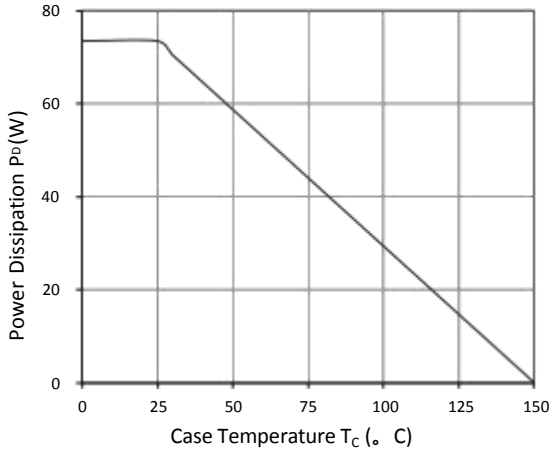


Figure 9. Power Dissipation

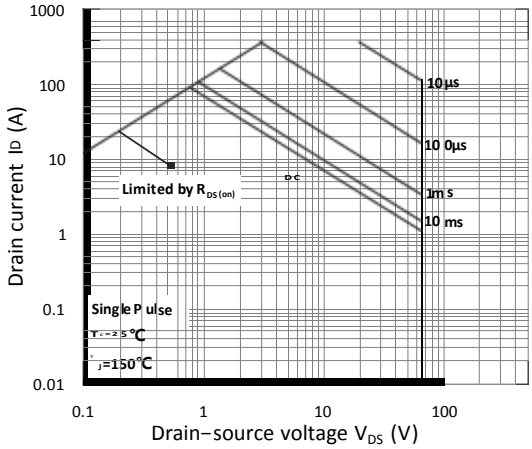


Figure10. Safe Operating Area

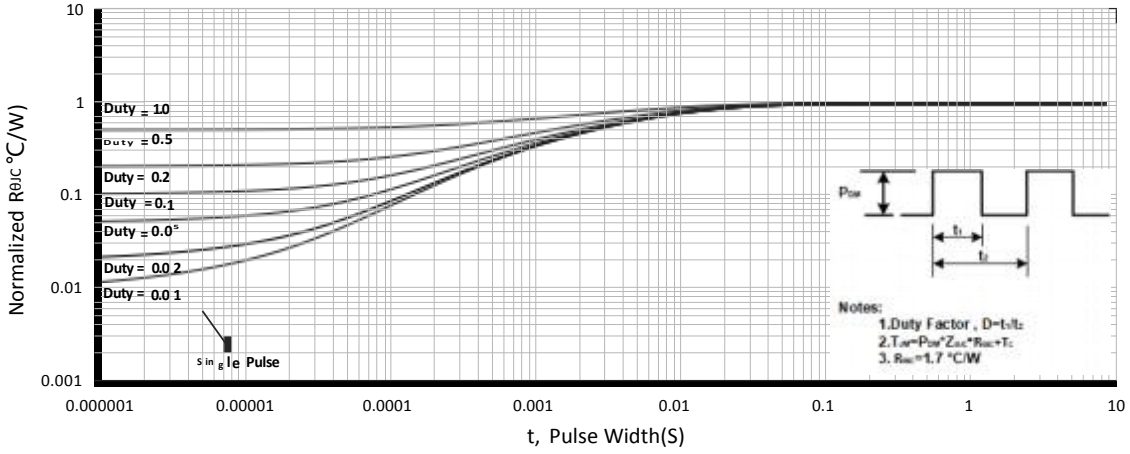


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

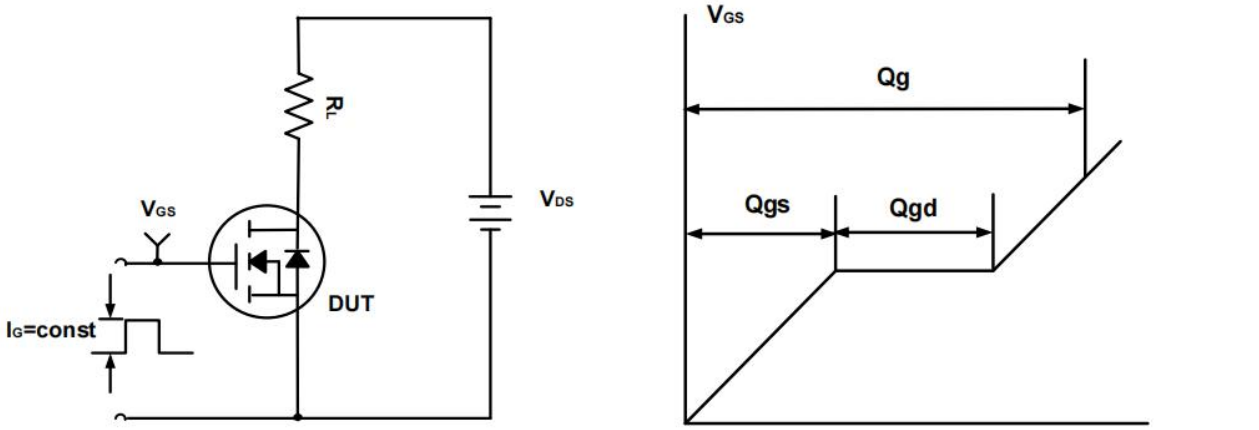


Figure A. Gate Charge Test Circuit & Waveforms

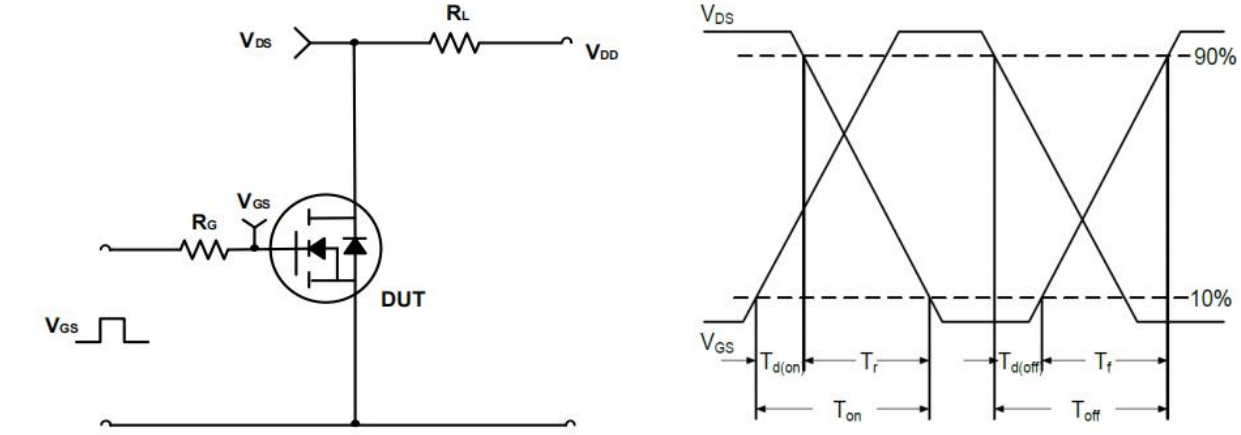


Figure B. Switching Test Circuit & Waveforms

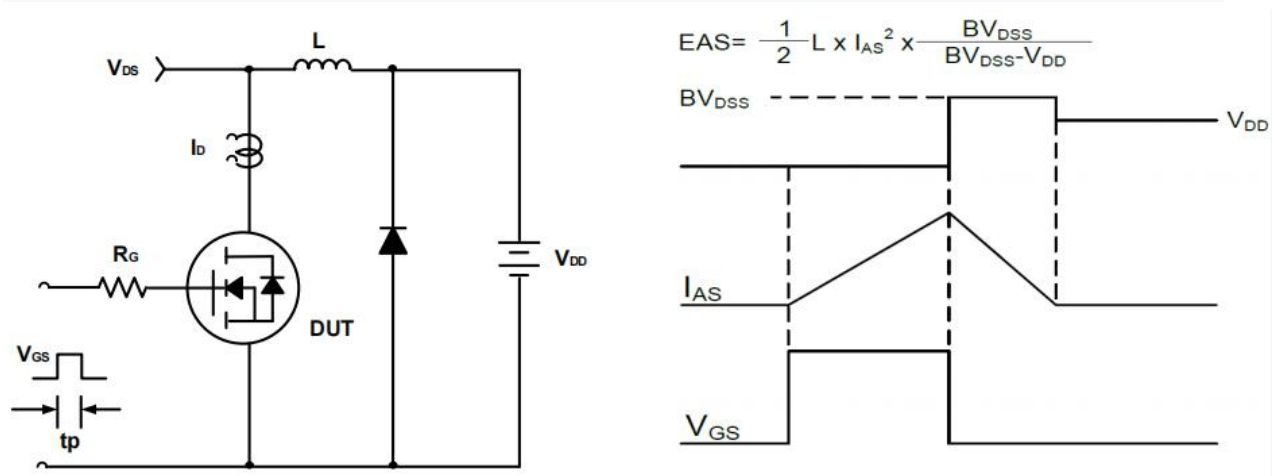
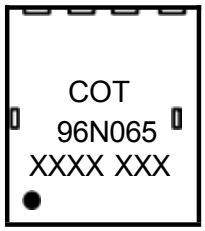


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Marking Information



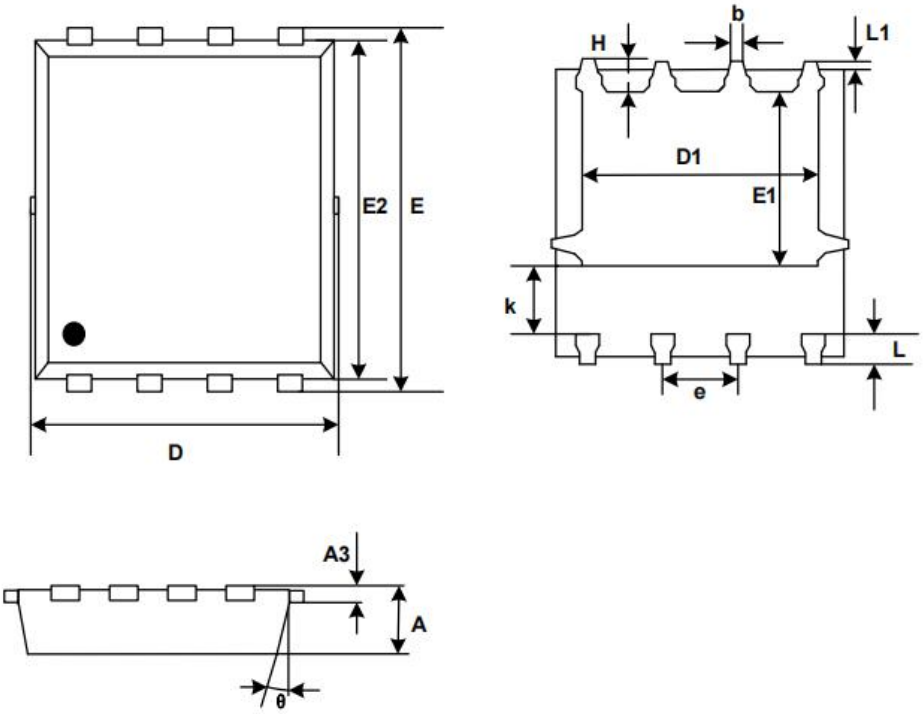
96N065= Device code

XXXX XXX= Date code

Package Information

Part	Package	Marking	Packing method
CT96N065ZC	PDFN5060-8L	96N065	Tape and Reel

Mechanical Dimensions for PDFN5060-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	0.90	1.20
A3	0.15	0.35
D	4.80	5.40
E	5.90	6.35
D1	3.61	4.31
E1	3.30	3.92
E2	5.50	6.06
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.71
θ	0°	12°