Description

This is -40V -50A P-Channel Enhancement mode power mosfet in a DFN3.3*3.3-8L plastic package.

CT50P04ZI uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

- Power Management Switches
- DC/DC converters

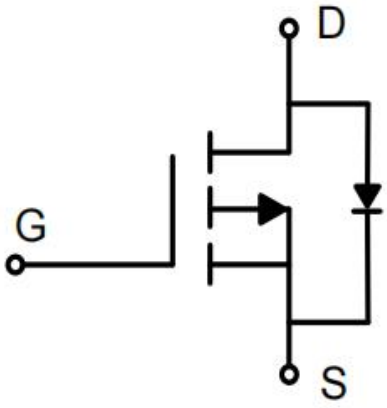
Features

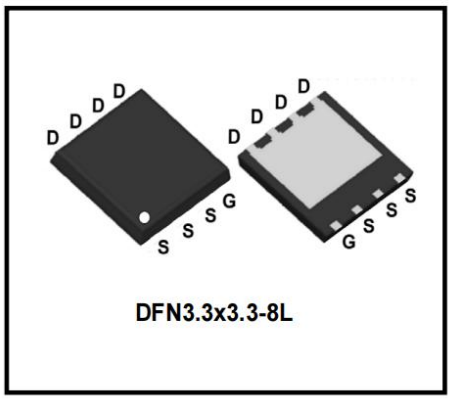
- VDS = -40V, ID= -50A
  RDS(on) < 8.5mΩ @ VGS = - 10V
  RDS(on) < 11mΩ @ VGS = -4.5V
- Green Device Available
- Low Gate Charge
- 100% EAS Guaranteed

V_{DS}	$R_{DS(on)(typ)}$	I_D
-40V	6.8mΩ	-50 A

Equivalent Circuit & Pinning

RoHS compliant





DFN3.3x3.3-8L

Absolute Maximum Ratings（TA = 25°C, unless otherwise noted）

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	-50	A
	T_C=100°C		-32	
Pulsed Drain Current[1]		I_{DM}	-200	A
Single Pulse Avalanche Energy[2]		EAS	125	mJ
Total Power Dissipation	T_C=25°C	P_D	35.7	W
Operating Junction and Storage Temperature Range		T_J , T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient[3]	$R_{\theta JA}$	56	°C/W
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	3.5	°C/W

Electrical Characteristics（TJ = 25° C, unless otherwise noted）

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-40	-	-	V
Gate-body Leakage current		I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T_J=25°C	I_{DSS}	V_{DS} = -40V, V_{GS} = 0V	-	-	-1	μA
	T_J=100°C			-	-	-100	
Gate-Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-1.6	-2.5	V
Drain-Source on-Resistance[4]		$R_{DS(on)}$	V_{GS} = -10V, I_D = -20A	-	6.8	8.5	mΩ
			V_{GS} = -4.5V, I_D = -15A	-	8.5	11	
Forward Transconductance[4]		g_{fs}	V_{DS}= -10V, I_D= -20A	-	104	-	S
Dynamic Characteristics[5]							
Input Capacitance		C_{iss}	V_{DS} = -20V, V_{GS} =0V, f =1MHz	-	5295	-	pF
Output Capacitance		C_{oss}		-	430	-	
Reverse Transfer Capacitance		C_{rss}		-	385	-	
Gate Resistance		R_g	f =1MHz	-	4.1	-	Ω
Switching Characteristics[5]							
Total Gate Charge		Q_g	V_{GS} = -10V, V_{DS} = -20V, I_D= -20A	-	110	-	nC
Gate-Source Charge		Q_{gs}		-	12.5	-	
Gate-Drain Charge		Q_{gd}		-	23	-	
Turn-on Delay Time		$t_{d(on)}$	V_{GS} = -10V, V_{DD} = -20V, R_G = 3Ω, I_D= -20A	-	16.8	-	ns
Rise Time		t_r		-	10	-	
Turn-off Delay Time		$t_{d(off)}$		-	65	-	
Fall Time		t_f		-	17	-	
Body Diode Reverse Recovery Time		t_{rr}	I_F = -20A, dI/dt= -100A/μs	-	42	-	ns
Body Diode Reverse Recovery Charge		Q_{rr}		-	29	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage[4]		V_{SD}	I_S = -20A, V_{GS} = 0V	-	-	-1.2	V
Continuous Source Current	T_C=25°C	I_S	-	-	-	-50	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
2. The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.4mH, I_{AS}= -50A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristic

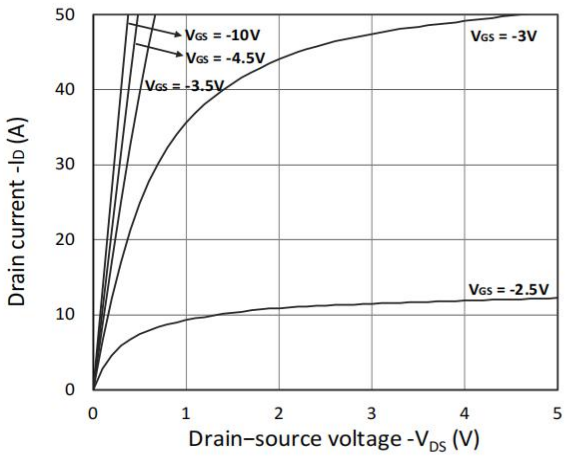


Figure 1. Output Characteristics

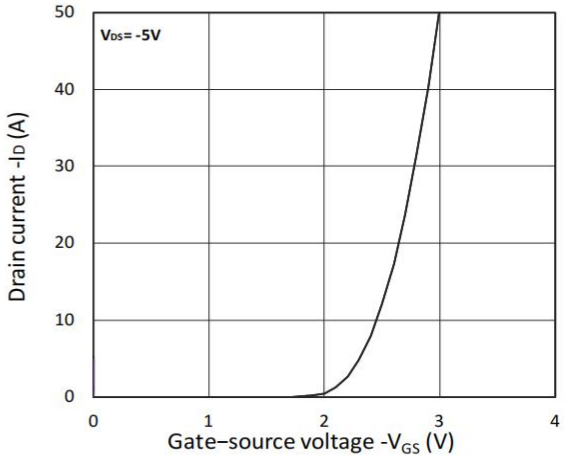


Figure 2. Transfer Characteristics

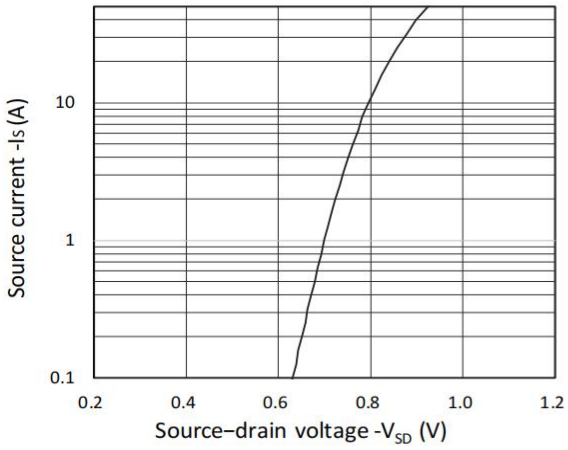


Figure 3. Forward Characteristics of Reverse

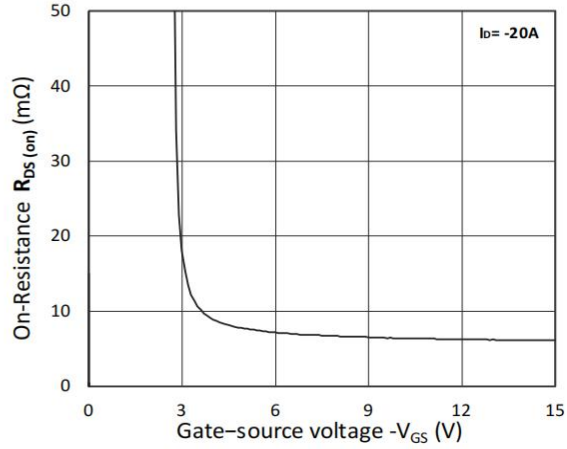


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

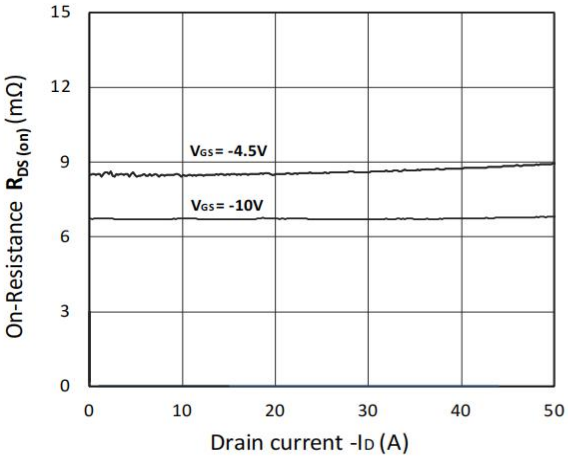


Figure 5. $R_{DS(ON)}$ vs. I_D

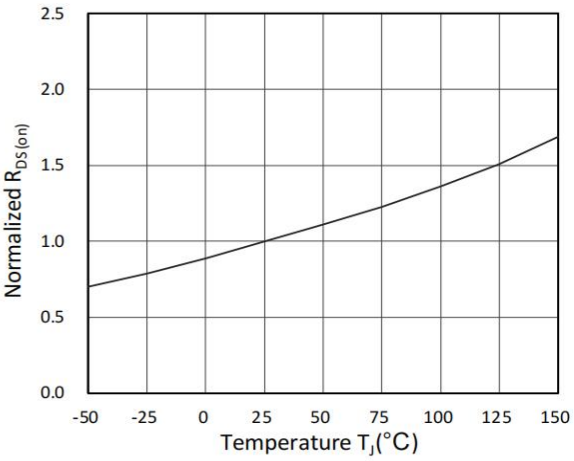


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

Typical Characteristic

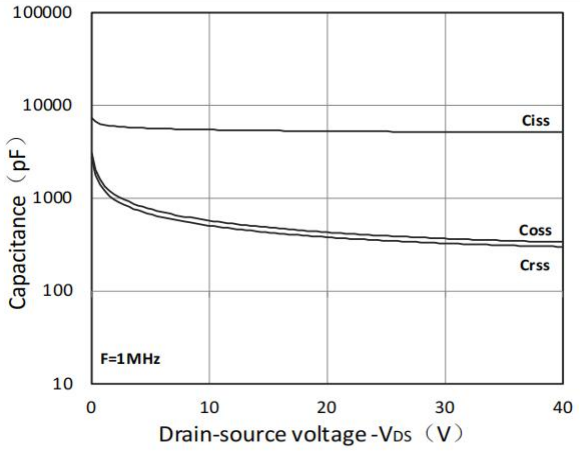


Figure 7. Capacitance Characteristics

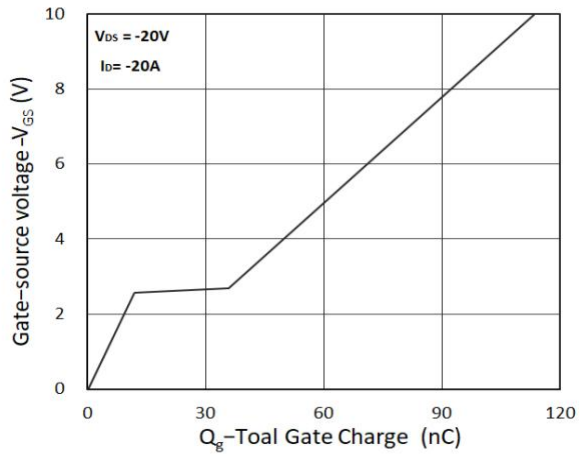


Figure 8. Gate Charge Characteristics

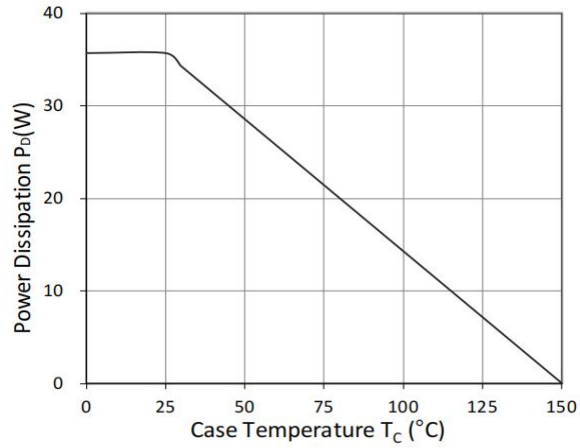


Figure 9. Power Dissipation

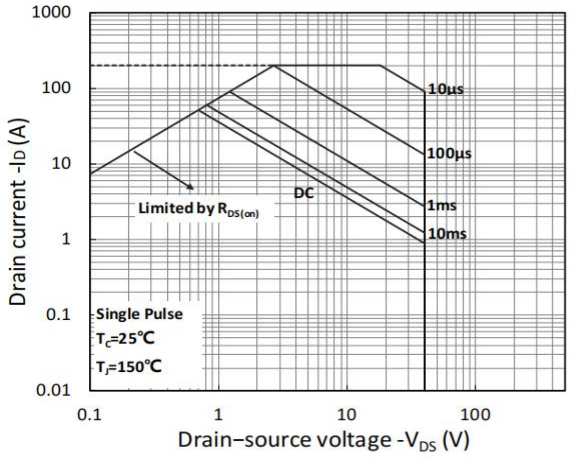


Figure10. Safe Operating Area

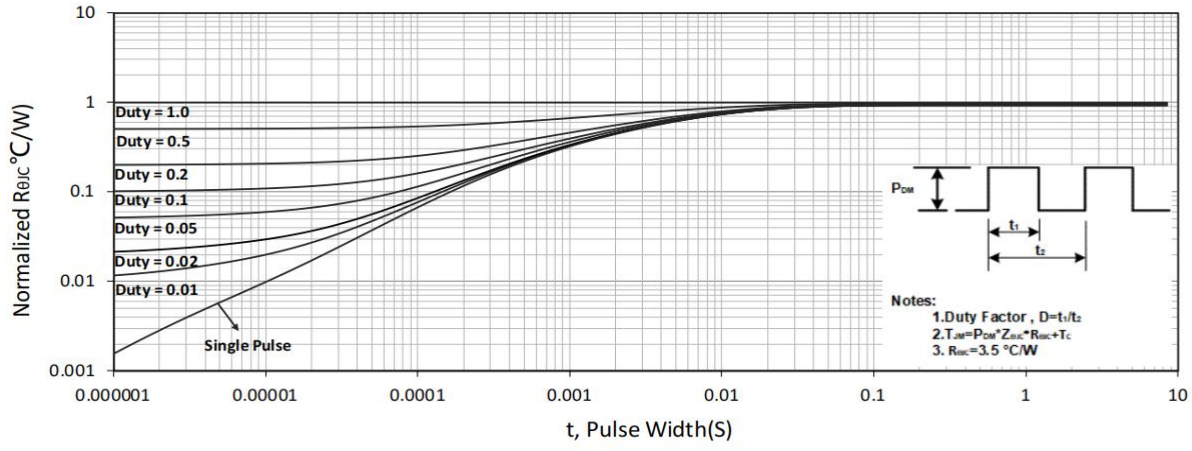


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

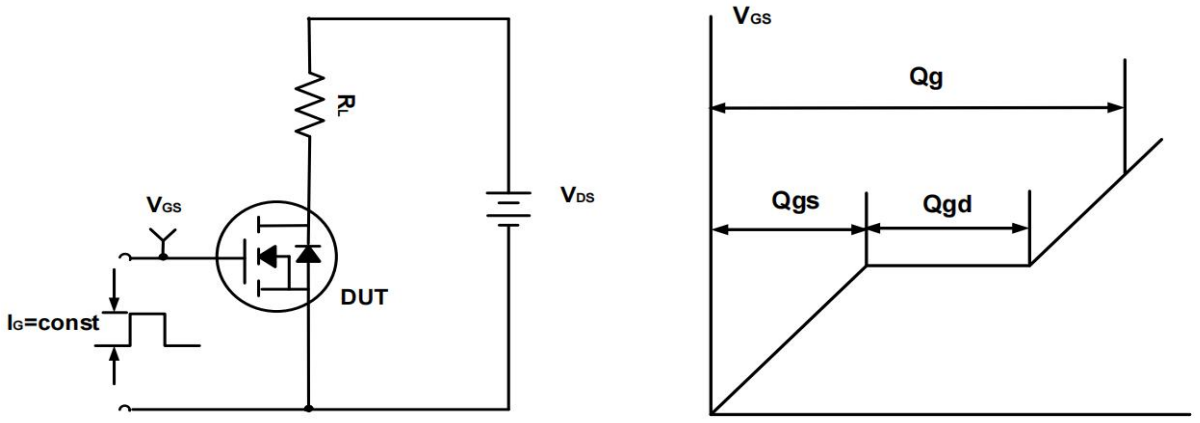


Figure A. Gate Charge Test Circuit & Waveforms

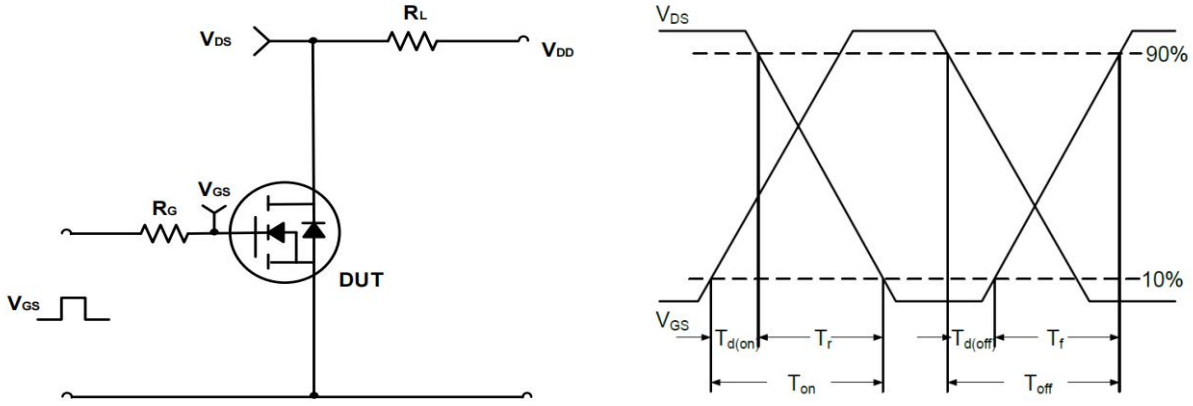


Figure B. Switching Test Circuit & Waveforms

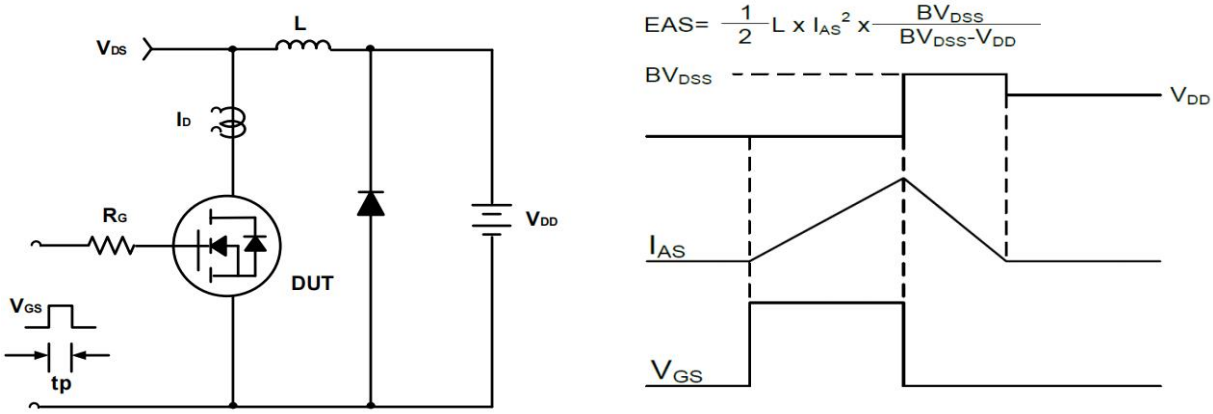
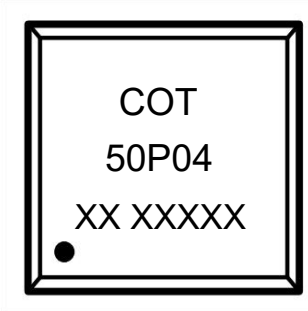


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Marking Information



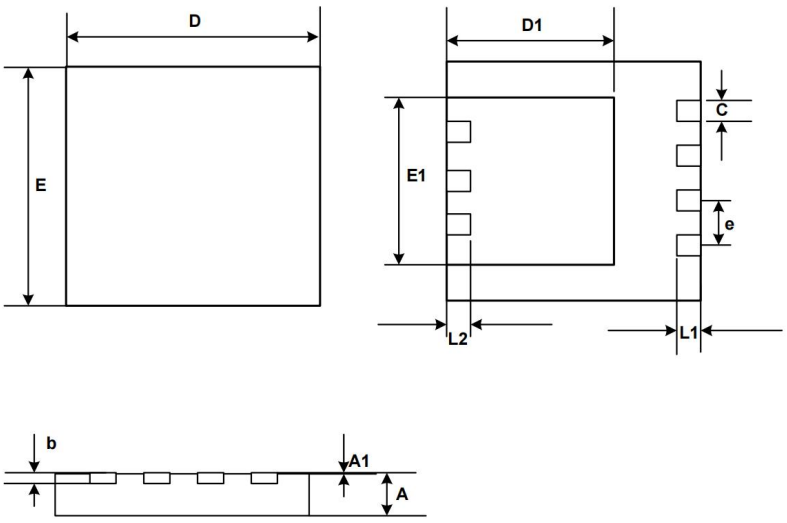
50P04= Device code

XX XXXXX= Date code

Ordering Information

Part	Package	Marking	Packing method
CT50P04ZI	DFN3.3x3.3-8L	50P04	Tape and Reel

Mechanical Dimensions for DFN3.3*3.3-8L



COMMON DIMENSIONS

SYMBOL	MM	
	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
b	0.216 REF	
c	0.290	0.390
e	0.65BSC	
D	3.200	3.400
D1	2.020	2.220
E	3.200	3.400
E1	2.190	2.390
F	0.405	0.605
L1	0.350	0.550
L2	0.300	0.500